ADVANCED 5G SUBSTRATES WITH INTEGRATED ANTENNAS

A Thesis

Presented to

The Academic Faculty

By

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In Partial Fulfillment

Of the Requirements for the Degree

Master of Science in Electrical and Computer Engineering

Georgia Institute of Technology

May, 2017

ADVANCED 5G SUBSTRATES WITH INTEGRATED ANTENNAS

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ACKNOWLEDGEMENTS

First and foremost, I would like to thank my advisor, Prof. Tummala for giving me the opportunity to do research at PRC, Georgia Tech. I would like to extend my most sincere thanks to my mentors: Prof. Manos, Dr. M. Raj Pulugurtha, Dr. Venkatesh Sundaram for their excellent mentorship and step-by-step guidance towards success. I have greatly benefited from their experience and their insights into the world of packaging. Especial credit go to Dr. Raj for his support at every step of this research. I would also like to thank my friends and colleagues: Atom Watanabe, Zihan Wu, Chandra Nair, Bartlet DeProspo, Matsuura Hiroyuki, Tomonori Ogawa, Dr. Fuhan Liu and the administrative staff of PRC for their help and support in smooth execution of this research work. You have been an invaluable source of knowledge and support. I would also like to thank my committee members for taking the time to study, understand and appreciate my research.

To my friends and family, thank you for your tremendous support and your faith in me to get through the challenges of work and life on the other side of the world. I am grateful for the sacrifices and the prayers that my parents made for me. It would not have been possible without your firm belief in me.

Lastly, I would like to thank the sponsors of this research and Qualcomm and PRC Research Group for giving me this excellent opportunity to improve and practice my knowledge.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

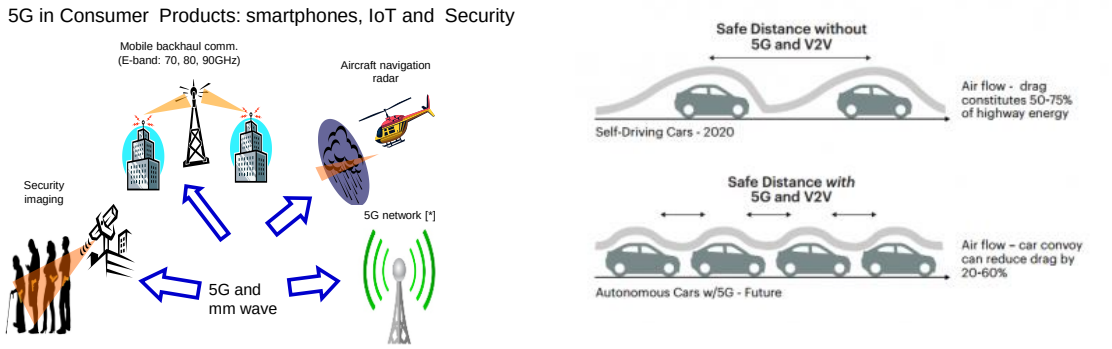
The objective of this research is to explore, develop and characterize advanced substrates for 5G applications in the frequency range of 26.5-40.0 GHz. Ceramic, organic laminates, wafer fan-out and glass substrates were compared against each other based on electrical performance, geometrical parameters and processability. Transmission line loss and patch antenna performance were used as the key electrical performance metrics. Model-to-hardware correlations were performed for the designed, fabricated and characterized test structures. The impact of process variations on the electrical response of patch antennas was also investigated.

1.1 What is 5G and why?

Fifth Generation wireless or mobile networks, abbreviated as 5G, are the proposed next telecommunication standards beyond the current 4G and LTE standards. This standard is based on mm-wave communications, which refer to electromagnetic signals with a wavelength of 1-10 mm millimeters in the frequency range of ~30 to 300 GHz. Wireless communications in 5G enable higher capacity than current 4G and LTE communication standards to allow higher density of mobile broadband users per area and support of ultra-reliable device-to-device and machine-to-machine communications.

There has been a growing demand in Radio Frequency (RF) applications in the last few decades, in applications such as sensing, detection, identification and communication applications. Examples of these applications include Gb/s local-area and wide area-networks, mm-wave automotive radar, imaging in the mm-wave and THz frequencies,

wireless senor networks, Radio Frequency Identification (RFID) and other multiple access communication systems. It is estimated that over 50 billion devices will be connected to the internet by 2020, in contrast to the current number (2017) of 28.4 billion devices. Moving towards 5G is a natural course, as higher data rates and high density of connected devices per unit area is the requirement from next generation of communication standard. The key system technologies enabled by 5G technology are classified as: (a) Wi-Fi Cellular and Backhaul Communications, (b) Vehicle-to-Everything (V2X) communications for Advanced Driver Assistance Systems (ADAS), (c) Internet of Things (IoT), (d) Massive MIMO, (e) Cognitive Radio. These are illustrated in Figure 1 and Figure 2, and discussed below.



(a) (b)

Figure 1: 5G applications for communications and automotive ADAS applications.

1.1.1 Wi-Fi, Cellular and Backhaul Communications

Cellular systems in 5G technology are in its early developmental stages with technology giants working towards introducing modems and similar communication devices in the market. The bands set for testing 5G cellular systems are 28 GHz in the US and 39 GHz in the Europe. The frequency ranges are 24.5 to 29.5 GHz and 37.0 to 43.5 GHz for the 28

and 39 GHz spectrum, respectively. Improved data rates of upto 2.5 Gbps with reduced latency and support of multiple connections are the key features of 5G cellular communications [1].

A relatively new Wi-Fi standard IEEE 802.11ad that operates in the 60 GHz band to achieve as much as 7 Gbps data transfer rate is also under development. This band can be used without a license for short-range communication. It was launched by the Wireless Gigabit Alliance back in 2009 and is poised to be an essential enabling technology with the increase in demand of bandwidth for applications such as gaming and HD video streaming. It is often termed as Wi-Gig due to its immensely fast data rates as compared to the current Wi-Fi standards operating at 2.4 and 5 GHz.

Other bands such as 71-76, 81-86 and 92-95 GHz bands are also used for high-bandwidth communication links as these frequencies do not suffer from environmental absorption. In case of the 92-95 GHz band, 100 MHz has been reserved for space-borne radios to limit this reserved range to a transmission rate of a few gigabits per second [2].

1.1.2 V2X communications for ADAS

The automotive industry is currently undergoing key technological transformations as the trends are strongly shifting towards self-driving cars requiring more and more vehicles to connect to the internet and to each other. In order to deal with real-time complex road situations, automated vehicles must rely on their own sensors but also work with the sensors around them whether they be on other cars or the roads themselves. These trends post a significant challenge to the underlying communication system as the information must reach its destination reliably within extremely short time frame. It is beyond the capability of current wireless technology to accomplish this. However, the next generation

of mobile communication technology holds promise to fulfill the challenges in latency, reliability, throughput in mobility and connectivity density. On the device and package levels, 5G technology has pushed the design and process engineers to investigate new methods to miniaturize sensors and other devices to operate flawlessly with high efficiency and reliability in a harsh environment such as a vehicle.

1.1.3 Internet of Things (IoT)

Internet of Things requires a confluence of technologies and standards such as actuators and sensors, wearable computing, communications and protocols, storage and computing infrastructure, network and varying data and analytics. Automation and integration of everything from entire factories to ubiquitous home appliances such as microwave ovens entail the transportation of bursts of data packets to and from large number of end-devices.

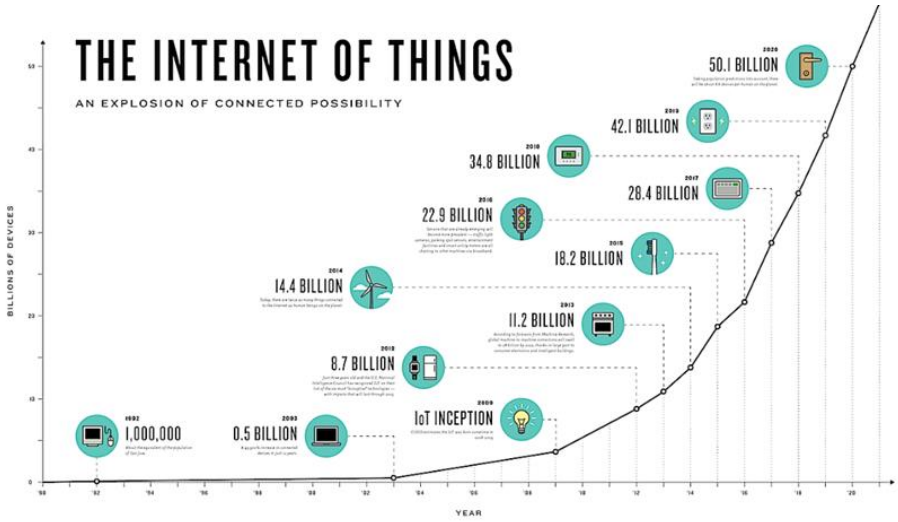


Figure 2: **Internet of Things: Prediction and history of connected umber of devices.**

The key aspects of machine-to-machine (M2M) communications on the network access are:

- Adaptable Quality of Service (QoS) support
- High integrity and energy saving
- Reduced latency
- Range of low to high communication bandwidth
- Significant increase in network and spectral efficiencies
- High system capacity, massive device connectivity
- Handling of small to large devices with varying traffic characteristics

All the above characteristics of M2M communication are to be addressed in the wireless next-generation network (NGN), which is to be introduced in the 2020 timeframe. It supports the need for high-density of devices based on small-cell configurations and access to network based on varying protocols and types of technologies. IoT with 5G technology provides the solution with increased bandwidth and higher spectral efficiencies to accommodate the magnitude of connectivity required by the requirements of near-future communication systems [3].

1.1.4 Massive MIMO

Massive Multiple-Input, Multiple Output (MIMO) transmission points are equipped with a very large number of antennas that can serve multiple users simultaneously [4]. With massive MIMO, multiple messages for several users can be transmitted on the same frequency resource, maximizing beamforming gain while minimizing interference [5]. Since mm-wave frequencies suffer from severe attenuation in indoor environments, massive MIMO antenna transmission points are needed to cover the increased density of users per unit area [6]. Several transmitting antennas can form a small cell, also known as a microcell, in a range of a few tens or hundreds of meters to provide faster data rates than

current 4G and LTE standards. Since the obstacle loss is significant at mm-wave frequencies, it will be inevitable to use beamforming techniques to utilize hundreds on antennas at base station. One such technique would be three-dimensional beamforming (3DBF), which will be utilized to steer the directional antenna beam to optimize performance metrics of the network [7].

1.1.5 Cognitive Radio

Smart radios, otherwise known as Cognitive radio technology, allows different radio technologies to share the same spectrum efficiently by finding unused spectrum adaptively and adjusting the transmission to the requirements of the technologies currently sharing the spectrum. This real-time radio resource management is achieved in a distributed fashion and relies of software-defined radio (SDR). Another domain in 5G is advanced interference and mobility management which is achieved with the cooperation of different transmission points with overlapped coverage. It encompasses the option to flexible use of resources for uplink and downlink transmission in each cell and the option to direct device-to-device communication with advanced interference cancellation techniques.

Systems with 5G connectivity impose several challenges associated with high-frequency design, losses and process control. Interconnection losses and impedance matching becomes extremely critical. Lumped components are not suitable for 5G. More complex distributed components with careful control in parasitics are needed. Attenuation at higher frequencies such as mm-wave spectrum is higher than that of lower frequency bands. Therefore, propagation is lossy in dielectrics and multipath propagation causes serious fading. A new class of substrate technologies are needed to comprehensively address all

these challenges and realize next-generation 5G systems, which forms the key focus of this thesis.

1.2 Research Challenges

Advanced Substrates

Typical parameters for the substrates are its electrical properties such dielectric loss and dielectric constant, dimensional stability with temperature and process conditions and CTE matching conditions to other layers of the package. Materials requirements for mm-wave are more stringent than for RF and digital applications. The primary reason for this is the sensitivity of mm wave performance to minor changes in properties. Along with the material properties, their performance is also sensitive to substrate geometries such as dielectric thickness, conductor width and roughness. A new class of substrate technologies with embedded actives, advanced antennas, and transmission lines with ultra-short interconnection lengths to actives are needed to realize 5G systems [8-10].

Low-Loss Transmission Lines

Transmission line insertion loss is used as the key performance metric for evaluating various substrate candidates. Insertion loss of a component is the loss of signal strength or power when it is inserted into a system. It is usually expressed in relative units: decibels (dB) or absolute units: dB power relative to 1 mW (dBm), dB power relative to 1 µW (dBµ). The challenge is to achieve a low loss of 0.05 dB/mm and the overall loss of the transmission lines including via transitions to not exceed by more than 3 dB. Another aspect of achieving this low loss is to control and minimize various contributing factors such as insertion loss such as radiation, dielectric and conductor and launching losses.

Model-to-Hardware Correlation Study

The discrepancy between model and hardware is a major challenge faced by both design and process engineers. At mm-wave frequencies, several challenges come into play. The wavelength corresponding to 40 GHz is just 7.5 mm and often, structures are designed to be a fraction of a wavelength. Slight variation due to process inconsistency can lead to a severe shift in the frequency response for the structures designed at mm-wave frequencies. Small variation can easily lead to a shift of few hundred MHz depending on the geometry of the structure. Improper launching of a signal into a structure can lead to unexpected results which can lead to damage to the system in case of active circuits.

1.3 Research Objectives

The objective of this research is to explore a variety of substrate options such as organic laminates, glass and ceramics and assess them for 5G applications based on their electrical performance and processability. The research is divided into three tasks:

1. Advanced Substrates with dielectrics and cores
2. Low-loss Transmission Lines
3. Model-to-Hardware Correlation with patch antennas

Table 1 shows the objectives, prior art, and challenges in each task.

Table 1: Research tasks with objectives, prior art and challenges.

Primary Task	Objectives	Prior Art	Challenges	Tasks to address Challenges
Advanced substrates	• Via parasitics: ○ 50 pH; 0.02 dB ○ 10 mm lines with 2% precision	• Via parasitics: ○ 140 pH; 0.03 dB ○ >40µm (laminates) with 5% precision • Laminates and LTCC	• Low Df substrates with stable characteristics in the desired frequency range • Dimensional stability for better lithographic ground rules	• Explore variety of substrate options to find suitable candidates for 5G at both substrate and package level
Low-loss transmission lines	• Loss <0.05dB/mm	• 0.09 dB/mm	• Minimize radiation, dielectric and conductor losses	• Low-loss laminates and glass with advanced build-up materials
Patch antenna design and characterization	• BW: 5% • Gain: 4 dBi • 2% process-variation	• BW: 3% • Gain: 3 dBi • 5% process-variation	• Discrepancy between model to hardware because of process variation, inaccurate properties, probing and calibration challenges	• Explore the use of multi-layer topologies and metamaterials • Process variation analysis

1.4 Brief Overview of Prior Art

State-of-the-art mm wave packages employ ceramics, organic laminates and fan-out packages with mold compounds. Examples of each are shown in Figure 3, and briefly described in this section. More details are provided in the literature review chapter. Ceramics are preferred for 5G applications because of their low loss, low moisture absorption, and stable properties in mm wave range and availability. The cost and integration limitations of ceramics led to the evolution of organic packages. A fully-integrated antenna-in-package (AiP) solution for W-band scalable phased-array systems is

demonstrated by IBM [11, 12]. A fully operational compact W-band transceiver package with 64 dual-polarization antennas was embedded in a multilayer organic substrate. Ultra-low loss organics based on Teflon and liquid-crystal polymers (LCP) were explored by VTT-Finland, with gains as high as 23 dBi and operational bandwidth of 2 GHz [11].

The evolution of embedded wafer fan-out packaging (EWFO), also referred to as embedded wafer-level ball grid array (eWLB) or fan-out wafer-level packaging (FO-WLP), further enhanced the performance or organic mm-wave packages. EWFO eliminates the use of wire bonding, which not only introduces significant radio frequency loss, but also increases the footprint for high-pin count die. Significantly reduced parasitics is the main advantage of eWLB compared to the standard BGA-wirebond and BGA flip-chip packages [13]. The transceiver bare die is embedded in a reconfigured molded wafer with compression molding process. Double-sided multiple redistribution layers are formed to fan-out the transceiver input/output signals, and through-mold vias are employed to realize the vertical interconnections. A fan-out eWLB with SiGe-BiCMOS technology was demonstrated by Infineon technologies [14]. Chang *et. al*., from IME Singapore, demonstrated a 3-D integrated 77-GHz automotive radar front-end [15].

For optimal performance, the patch antenna topologies typically need to be integrated on the substrate with active circuits using low-loss interconnects and feedlines [10-12]. State-of-the-art mm-wave modules cannot handle precision and tolerance for mm-wave components approaching the dimensions of a few microns. Glass-based packages are emerging as ideal candidates to realize mm-wave technologies because of their superior dimensional stability, availability in large-area low-cost panels, ability to form fine-pitch through-vias, stability to temperature and humidity, and matched coefficient of thermal

expansion (CTE) with devices [16], along with low dielectric loss compared to silicon and mold compounds used in fan-out packages. Projected performance of glass substrates is qualitatively compared to other substrate options in Figure 4. Prior art of each task is discussed in detail in Chapter 2.

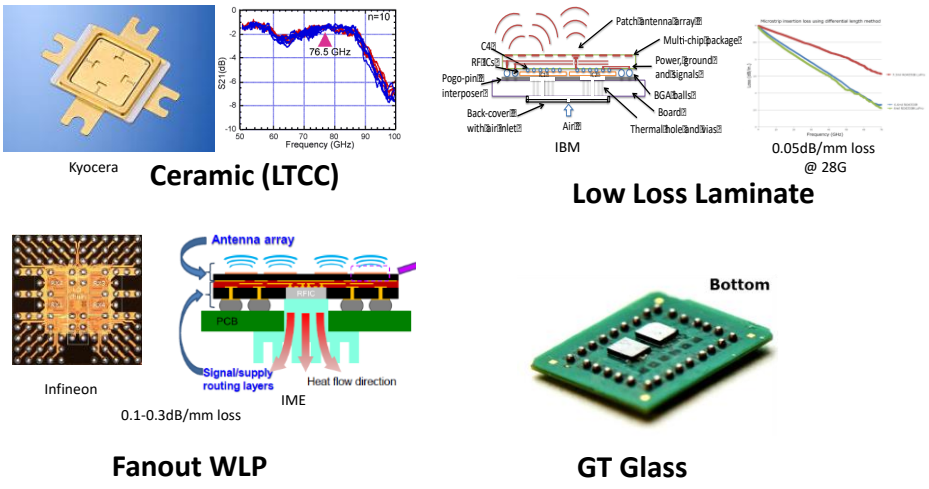


Figure 3: Current 5G ceramic, organic, fanout and glass substrates.

1.5 Proposed Research Tasks

Advanced 5G designs and innovative 3D structures with fan-out or double-side assembly, aided by fine-pitch through-vias and precision multilayered fine-line RDL are required to harness the benefits of glass and other advanced substrate technologies, which forms the key focus of this thesis. Three research tasks are proposed to address the challenges mentioned above and accomplish the objectives discussed in Table 1. The tasks along with their details are briefly explained below.

5G Attribute	Ceramic	Laminate	FO WLP	GT GFO
Material Loss				
Total Electrical Loss				
Precision RDL				
Large panel				
Fine pitch				
Thin form factors				
Antennas				

Figure 4: Qualitative comparison of various substrate options for 5G applications

(Image Courtesy: Dr. Venkatesh Sundaram, Georgia Tech)

1.5.1 Advanced Substrates

The objective of this task is to develop and characterize next-generation 5G substrates with via transition loss less than 0.02 dB, transmission line loss less than 0.05dB/mm and interconnection parasitics of less than 50 pH and 10 milliohms. Typical feature sizes for mm wave transmission lines and via transitions can be as low as 5 µm, which naturally brings out the need for lower substrate losses and consistency over the desired band of operation. The significance of material properties can be illustrated through an analysis of various contributions to insertion loss.

1.5.2 Low-Loss Transmission Lines

Low-loss transmissions with innovative waveguide structures on glass and advanced organic substrates will be modeled, designed and demonstrated to achieve insertion losses approaching 0.05 dB/mm. Advanced low-loss materials with low Dk, Df and stable characteristics in the desired frequency range will be used as the build-up materials. Low-

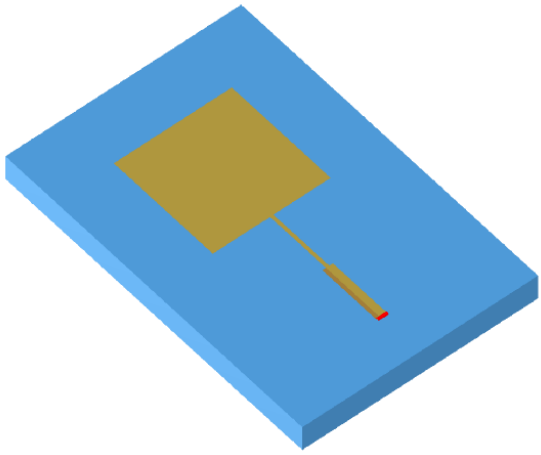


Figure 5: A typical patch antenna.

loss transmissions with innovative waveguide structures on glass substrates will be utilized to achieve low insertion losses. Precision circuitry will be enabled by high dimensional stability and surface smoothness of glass, resulting in further lowering of the losses from impedance mismatch.

1.5.3 Model-to-Hardware Correlation Study

The objective of this task is to investigate the validity of 5G models and quantify the effect of process variation on performance deviation. Single-element patch antenna at a frequency of 39 GHz was selected for this study. A typical patch antenna structure is shown in Figure 5. The choice of structure for this study serves another purpose as well. A single-element patch antenna is sensitive to its longitudinal dimension. Resonant frequency can dramatically vary with this length. The variation of resonant frequency from process variation can be studies from this task. Glass substrates from Asahi Glass are utilized for the demonstration.

Semi-Additive Process (SAP) is used to fabricate feedline network patterns and patch antennas on a substrate panel. This study with reveal the degree of dependence of this design and its corresponding variation upon testing.

In summary, advanced substrates for 5G substrates using three sets of performance metrics: low-loss transmission lines, patch antenna performance and impact of process variation are investigated. Both core and buildup layers are considered, leading to recommendations for an ideal candidate for 5G applications.

CHAPTER 2

LITERATURE REVIEW

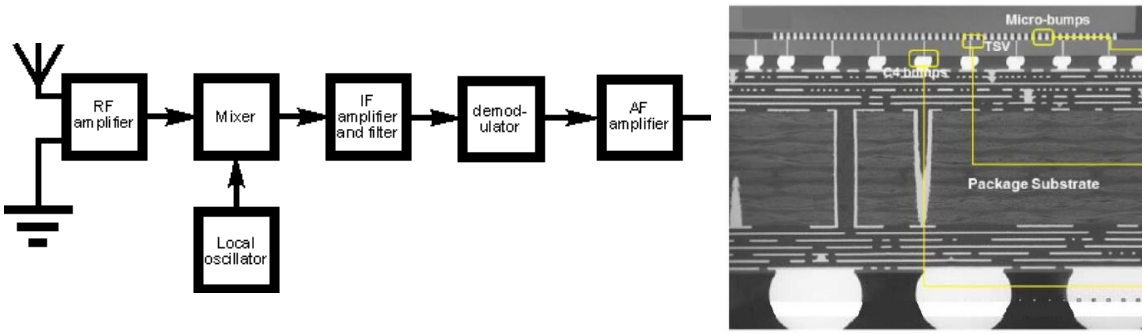
This chapter reviews various building block technologies for 5G applications. It is organized as follows: a typical 5G system along with its components is discussed. Several technological advances such as transistors, interconnects, antennas and passives related to 5G systems are presented in detail. State-of-the-art and emerging variants of each technology are also discussed. Major emphasis of this chapter is placed on substrate technologies, typical substrate structures and fabrication processes:

2.1 5G System and its Components

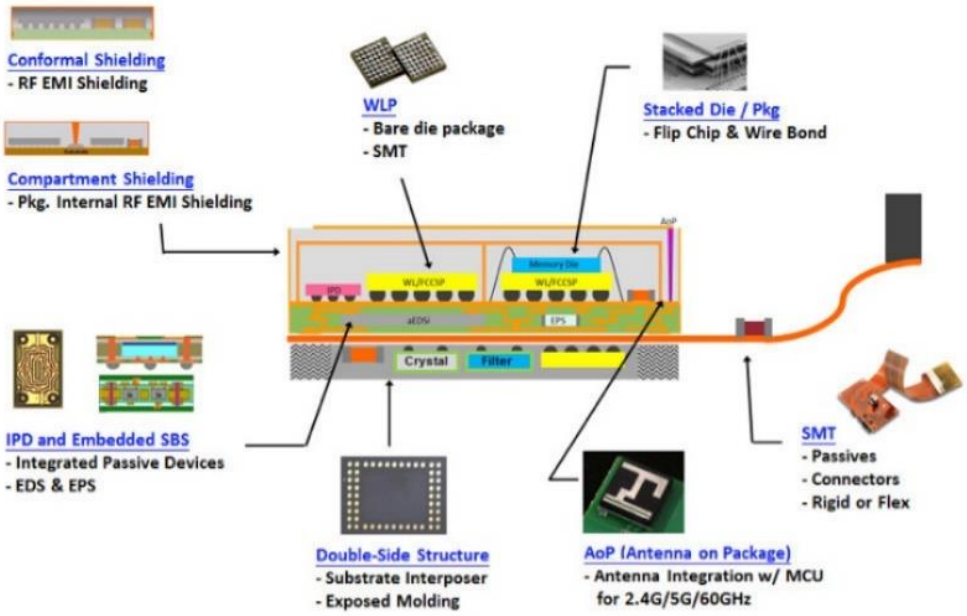
A highly-integrated 5G substrate system architecture along with traditional discrete module is shown in Figure 6. Following system components are an integral part of a 5G substrate system:

- Integrated Circuits (ICs)
- Transmission Lines
- Passives
- Antennas
- Interconnects
- Substrates (Core and Buildup)

These components of the 5G substrate system are discussed in detail in the following sections.



(a) (b)



(b)

Figure 6: Conceptual 5G substrate system (a) example of a front-end module architecture (b) traditional substrate and components, (c) Emerging highly-integrated fan-out packages.

2.2 Integrated Circuits (ICs) for a 5G System

Several advanced transistor technologies come into play for mm-wave applications and are thus suitable options for 5G systems. Most mm-wave circuits have been implemented in Indium Phosphide (InP)-based or Gallium Arsenide (GaAs)-based transistor technologies.

High Electron Mobility Transistors (HEMTs) have been historically used for high-speed applications because of their relatively higher current gain cut-off frequency and maximum oscillation frequency. In recent years, InP-based Heterojunction Bipolar Transistors (HBTs) deliver superior performance to any other transistors. However, Silicon Germanium (SiGe) and BiCMOS (integrated bipolar junction transistor and CMOS transistor in a single integrated device) are challenging InP-based transistors for mm-wave markets and have ability to integrate high degree of functionality in a single chip [17, 18]. After the year 2000, silicon-based technologies gradually took over GaAs-technologies. This is because they have much better integration capabilities as compared to GaAs. It is easier to integrate the baseband digital circuits into a single chip with mm-wave circuits in Si-based technologies rather than that in GaAs-based technologies [19]. Infineon technologies has proposed a SiGe BiCMOS for automotive radar solutions in 76-81 GHz [14]. This radar is based on Monolithic Microwave Integrated Circuit (MMIC) technology. Better performance of the SiGe HBTs is needed to improve performance as this technology has cutoff frequencies in the range of 200-300 GHz, which is only a factor of 3 higher than the application frequency, resulting in lower margin for RF design. Infineon's SiGe BiCMOS technology can improve the RF performance and address the limitations in SiGe HBTs.

Systems with 5G standards have been challenging leading device companies to mass-produce low-cost ICs. Qualcomm, a leading organization in the world of communication, recently announced its 28 GHz 5G Chip [20]. It is a modem operating at 28 GHz and it will be used for testing pre-standard 5G cellular trials by Verizon and Korea Telecom. This indicates the roll-out speed of some vendors to push 5G standard even closer in time.

The Snapdragon X50 has the capability to deliver 5 Gigabits per second (Gbps) downlinks and multiple gigabit uplinks for mobile and fixed-wireless networks. It also has a separate LTE connection as an anchor for control signals, whereas the 28 GHz link can deliver higher data rates over tens to hundreds of meters. It features eight 100 MHz channels, a 2×2 Multiple Input Multiple Output (MIMO) antenna array, adaptive beamforming techniques and 64 Quadrature Amplitude Modulation (QAM) to achieve a 90-dB link budget. It is compatible with other Qualcomm chips such as SDR05x mm-wave transceiver and PMX50 power management chip. These transceivers have evolved over time to achieve higher data rates and excellent power management. With the advancements in technology, most of the supporting passives are also included in ICs to save package real-estate and utilize it for some other purpose such as heat management or increase density of components on it. A typical transceiver architecture is shown in Figure 7. This brings a very interesting perspective in the 5G substrates domain. Since the integration at circuit level is advancing with components being moved from the package to the IC itself, the main purpose of package has moved from supporting external components to provide high fidelity and low-loss interconnects to effectively route the IOs of the IC.

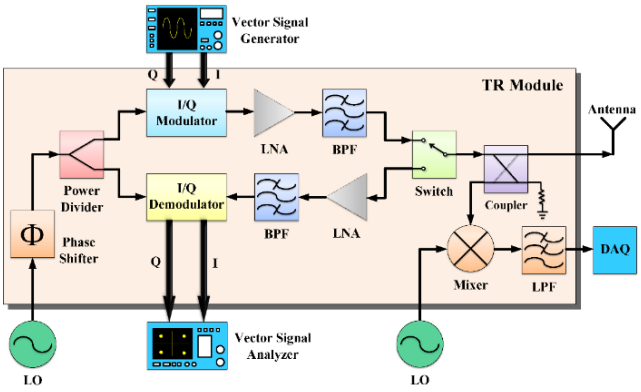


Figure 7: Microwave/mm-wave transceiver system with high-speed data rates for 5G.

2.3 Transmission Lines and Passive Components

Transmission Lines

For 5G packages, typical transmission lines such as microstrip, stripline and conductor-backed coplanar waveguide (CBCPW) are common. Stripline is usually avoided due to its higher loss. CBCPW and its ground-less variant, CPW, are profusely deployed due to their inherent shielding features and comparative losses to that of a microstrip transmission line. These transmission lines with their cross-sections are shown in Figure 8. In case of multilayered packages with less or no shielding between the layers, CPW is the line of choice. Usually, high-power signals in the system are routed through CBCPW lines to avoid any coupling with adjacent lines and compromising the signal integrity.

Above 30 GHz and at mm-wave frequencies, microstrip suffers from increased radiation loss and problems with spurious propagation modes which are undesired to maintain signal integrity. Often, the designers choose to transition from microstrip to CBCPW as soon as physically possible to avoid radiation loss and benefit from minimal spurious mode propagation. Another advantage of using microstrip and CBCPW is their exposure which

helps in assembling surface mount devices (SMDs) on them. These transmission lines also provide ease of testing along with lower fabrication cost.

Striplines become unattractive due to its small dimensions, higher losses and difficulty in routing using vias. Moreover, it is difficult to fabricate as compared to microstrip and CPW, and usually avoided at mm-wave frequencies. Achieving close-to-ideal transitions from stripline to coaxial or any other transmission line is also a challenge. However, stripline is not a lost art as it can be used at mm-wave frequencies when paired with the appropriate

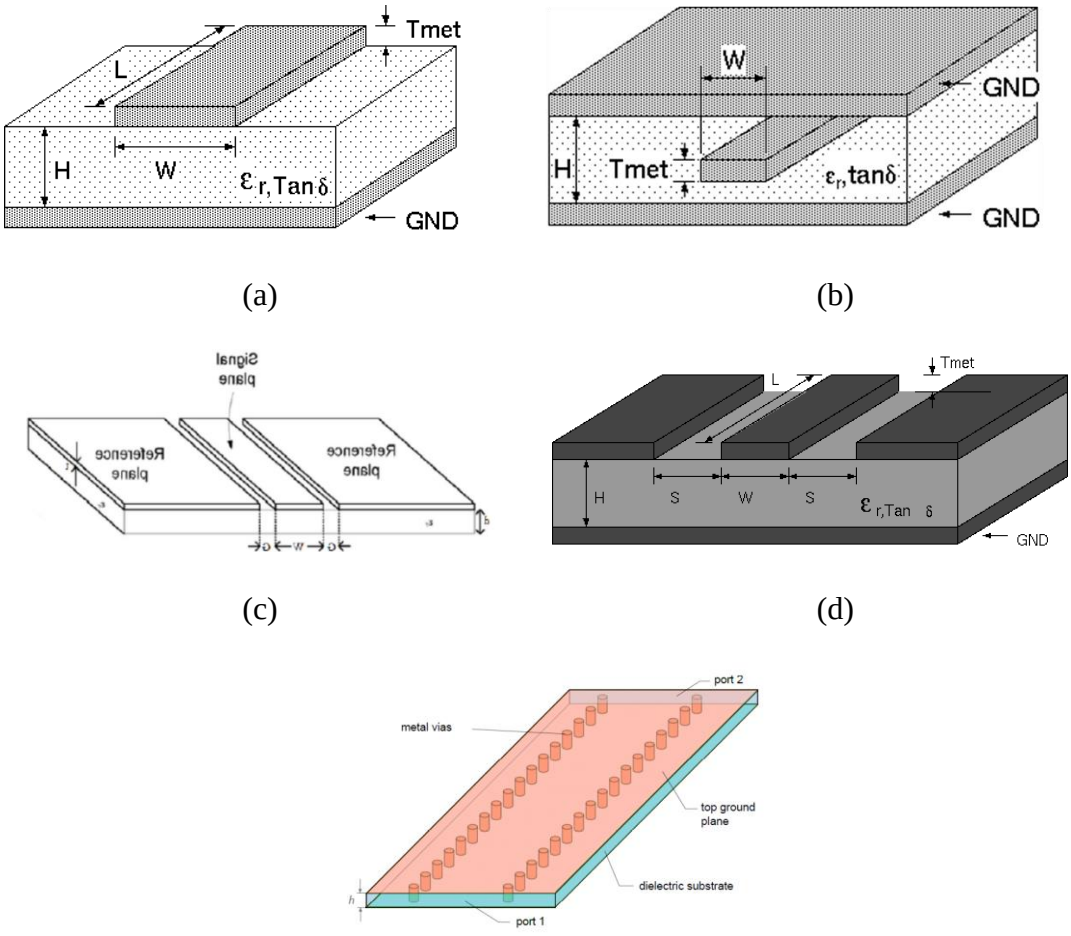


Figure 8: Transmission Lines (a) Microstrip (b) Stripline (c) CPW (d) CBCPW (e) SIW.

materials. Suspended Stripline structures can be a suitable option for two-layered substrate systems but it has limited applications in 5G systems.

Substrate Integrated Waveguide (SIW) is an embedded waveguide created within a substrate. Essentially, it is a dielectric-filled rectangular waveguide with reduced height, that is, the height of the substrate. The side-walls of this waveguide are created with arrays of plated via holes. It is shown in Figure 8(e). This makes it a very attractive option for passive devices and signal routing, given that it is less costly to fabricate. Moreover, it has the same characteristics as a conventional rectangular waveguide. SIW is a relatively new transmission line as compared to its counterparts and many innovative techniques to develop passive components using it have been published, especially filters because of its inherent structural flexibility in coupling design and topological arrangement [21].

Passive Components and Devices

Passive components such as resistors, capacitors and inductors are universally found in every PCB. Initially, larger size through-hole passive components were used in circuit boards but with the advancement in technology to using higher frequencies for circuits, passive components needed to be evolved as well. Once the operating wavelength of the system becomes comparable to the size of the components, several parasitics come into play. A resistor might depict capacitive properties due to its enclosure, causing unnecessary capacitance in the system. To avoid these parasitics, component size is made smaller than $\lambda/10$ of the operating frequency. Since the components at RF frequencies (upto 20 GHz) are very small, through-hole technology is no longer suitable for them. Surface Mount Technology (SMT) is the method of producing electronic components in which the

components are directly mounted onto the surface of PCBs. The passive SMT components fall in the category of surface mount devices (SMDs).

The process of reflow soldering is used to mount SMDs on a PCB. Since SMDs are suitable for high-volume production at a low cost, they are very popular among PCB designers as the cost of assembly also decreases with the increased production volume of these devices. At mm-wave frequencies, even SMT falls short as the parasitics overwhelm the actual properties of the component. A capacitor can behave as an inductor at higher operating frequencies. At mm-wave, usually the passives are avoided or are realized using active devices such as a diode-connected transistor acting as a resistor. Another approach is embedded passives where the passive components are made using conductor patterns and are embedded in a multilayered package. Figure 9 depicts the concept of embedded passives for a LTCC package.

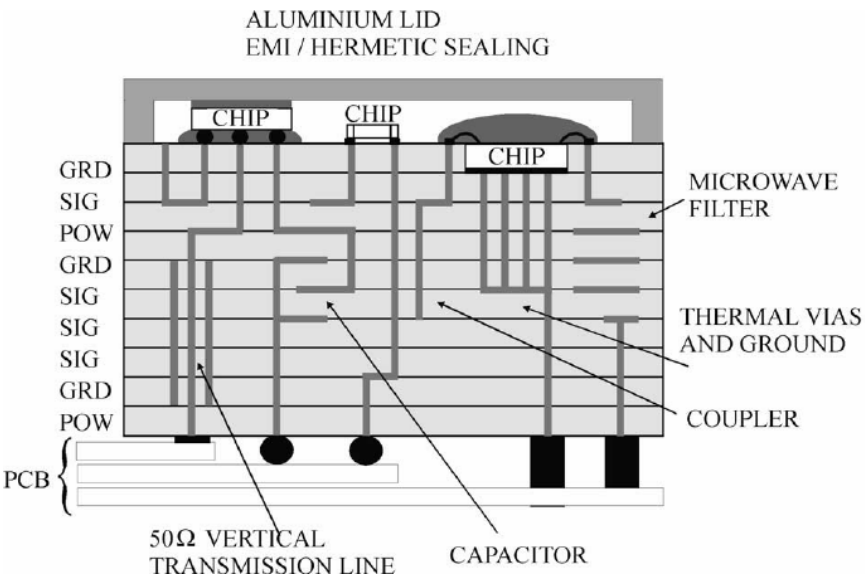


Figure 9: LTCC cross-section as an illustration of embedded passives.

Embedded passives have the following advantages [22]:

- Increased circuit density by saving real-estate on the substrate
- Decreased product weight
- Improved electrical properties through additional termination and filtering opportunities, and shortening electrical connections
- Cost reduction through increased manufacturing automation
- Increased product quality through elimination of incorrectly attached devices
- Improved reliability through the elimination of solder joints

Embedded passives, however, have a disadvantage in terms of the quality factor of the component, mathematically defined as:

$$Q = \frac{f_r}{\Delta f} \tag{1}$$

where f_r is the resonant frequency and Δf is the resonance width or bandwidth of the system.

An ideal passive component has infinite Q-factor.

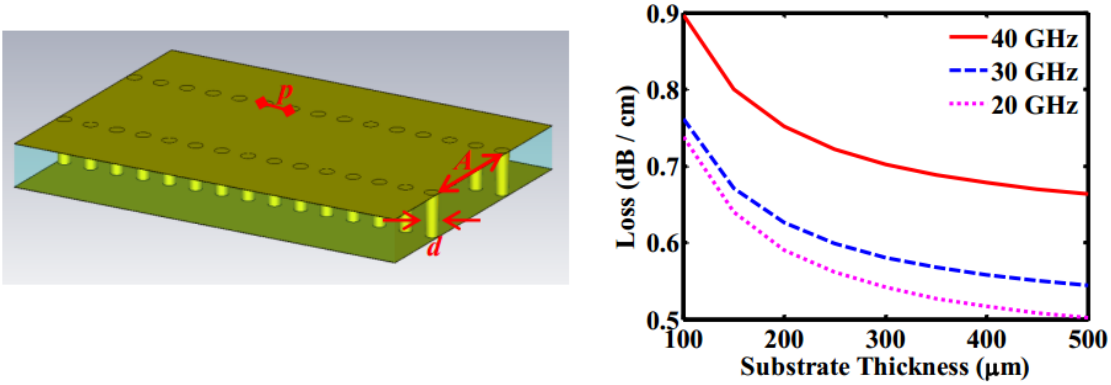
Embedded passives, especially inductors, suffer from poor Q-factor at RF frequencies and, therefore, are avoided by circuit designers when operating at frequencies over 20 GHz. Capacitors, on the other hand, can be embedded and made to have higher Q. Typical embedded capacitor structure is of a parallel-plate capacitor. As shown in Figure 9, embedded passives not only refer to resistors, capacitors or inductors, but also can be transmission lines, filters, couplers and even vias.

J. H Lee et al., report several mm-wave passive components using 3D LTCC system-on-package (SOP) technology [23]. His work reports slotted-patch resonator as a filter,

duplexer at 41/61 GHz, three- and five-resonator bandpass filter (BPF) at 60 GHz and a 40 GHz directional filter. Another work by F. Aryanfar et. al., reports a compact mm-wave filter using capacitively loaded CPW resonators at W-band [24]. They used the method of loading a CPW line with multiple capacitive loads along the length of the transmission line to increase its capacitance. They also provide a hybrid method of simulation by combining method of moments (MOM) and circuit simulations which facilitates a systematic approach for filter design at mm-wave frequencies. Z.C. Hao et al., report development of a low-cost W-band CQ BPF integrated with fine-line SIW-waveguide transitions on an organic laminate (Rogers RO5880) with loss tangent of 0.0009 at 10 GHz [25]. It is a coupling structure with a fractional bandwidth of 2.5% centered at 80 GHz. This demonstration reveals that low-cost commercially available substrates can be used for the fabrication of mm-wave passive devices. Similarly, a mode suppression technique for microwave and mm-wave LTCC filters using discriminating coupling is reported in [26]. The author proposes a new discriminating coupling mechanism, which is realized by choosing suitable coupling region between the feeding lines and resonators, and it suppresses the unwanted resonance modes without affecting the desirable operating modes. Using this technique, a BPF is designed at 60 GHz in LTCC structure by suppressing the fundamental mode.

J. Tong et. al. of PRC Georgia Tech reports a SIW in glass interposers using through-package-vias (TPVs) [21]. The SIW was designed at an operating frequency of 20 GHz with a 100% fractional bandwidth and 0.67 dB/cm insertion loss on a 130 μm glass. The diameter of vias, denoted by d, is set at 120 μm. The study also showed that the insertion loss in dB/cm decreases with increasing substrate height. Figure 10 shows the designed SIW and loss in dB/cm. Insertion loss varied over 1% when via diameter was changed from

100 to 480 μm, indicating that radiation loss in minimized due to the relatively small via diameter. This study indicates that glass is an ideal package substrate for mm-wave systems.



(a) (b)

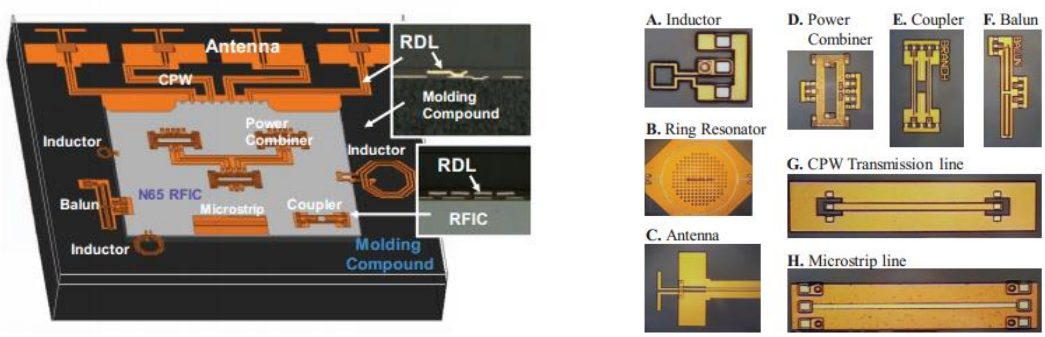
Figure 10: (a) Designed SIW (b) Loss in dB/mm vs. substrate thickness.

Image Courtesy: J. Tong, Georgia Tech

C.H Tsai et al., at TSMC realized high performance passive devices for mm-wave system including inductor, ring resonator, power combiner, coupler, balun, transmission line and antennas using integrated fan-out (InFO) WLP [27]. The inductors have a Q factor of over 40 and the power combiner, coupler and balun show lower transmission loss than on-chip passives. The schematic and fabricated passive devices are shown in Figure 11.

2.3 Antennas

Antenna is a very important part in a communication system as it is the interface between electrical and electromagnetic world. A better design antenna can add flexibility to the trade-offs between various parameters in a communication system by relaxing the stringent



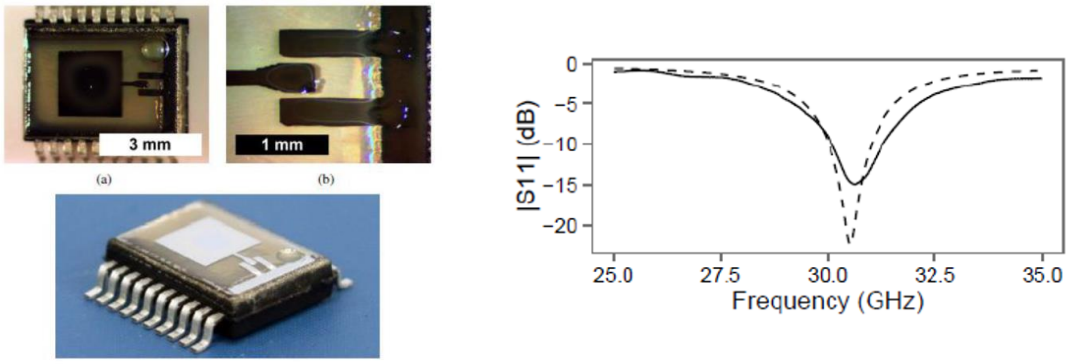
(a) (b)

Figure 11: (a) Schematic of mm-wave circuit including RFIC, passive devices and antennas (b) realized passive devices.

Image Courtesy: C.H. Tsai, TSMC

requirements. Massive MIMO and mm-wave technologies are considered to be the key technologies for 5G wireless communications. Moreover, the antennas for 5G would be combined in the form of arrays to achieve higher gain and directivity and will have phase-shifting capabilities to align their beams in the direction of maximum power reception. The key design parameters for antennas operating at 5G bands are high gain, high directivity, MIMO, planar in nature, small size and the ability to withstand harsh environments with minimum variation in performance over a large range of changes in ambient conditions.

Major advances have been reported on antennas at mm-wave frequencies, especially at 60 GHz and 75-81 GHz band. On-chip and on-package integrated antennas are also a key feature of 5G communication antennas [28]. Figure 12 shows an antenna fabricated after the chip is processed and has an operating frequency of 30 GHz. An aperture-coupled patch antenna integrated with a soft surface and a stacked cavity has been demonstrated on LTCC multilayer technology by J.H Lee et. al [29]. It has a higher gain of approximately 7.6 dBi, which is achieved by stacking the cavity underneath the soft surface. It was also confirmed that the back radiation is significantly reduced by about 2.5 dBi by stacking cavity to the



(a) (b)

Figure 12: (a) On-Chip fabricated rectangular patch antenna, and (b) its return loss.

Image Courtesy: B.K. Tehrani et.al, Georgia Tech

patch antenna with the soft surface. The antenna has the capability to be integrated into 3D 60 GHz modules and it can be easily extended to array configurations for point-to-point applications in short-range indoor wireless personal area network (WPAN). The antenna is shown in Figure 13 with its response.

So far, only broadside antennas (antennas with radiation pattern normal to the plane of the antenna) were discussed. Another class of antennas which have their beam in-plane to the antenna are known as end-fire antennas. Yagi-Uda antenna is one of the most common end-fire planar antennas. They are basically dipole antennas with directors to enhance their directivity. An important feature of a Yagi-Uda antenna is its limited dependence of the substrate used for its fabrication as most of the fields are concentrated in the dipole and the directors, therefore making it an ideal choice for end-fire antennas with ultra-thin substrates.

(a) (b)

Figure 13: (a) LTCC patch antenna, and (b) its return loss.

Image Courtesy: J.H. Lee et.al, Georgia Tech

B.K Tehrani et al., report a Yagi-Uda antenna with high-gain for use within the 24.5 GHz ISM band, realized through a multilayer, purely additive inject printing fabrication process on a flexible LCP substrate with 120 μm thick dielectric substrate. The antenna has an end-fire gain of 8 dBi and is low-cost, has the capability of being vertically integrated for on-chip and on-package integration. Figure 14 shows the antenna layout and its fabricated version. These antennas can also be made to have over 10% fractional bandwidth to cover a wide range of frequencies for 5G applications such as Gigabit wireless networks, automotive radar and biological imaging at 28, 39 GHz and beyond.

(a) (b)

Figure 14: Planar Yagi-Uda antenna (a) layout (b) fabricated version.

Image Courtesy: B.K. Tehrani et.al, Georgia Tech

Y. Li et al., report a low-cost high-gain and broadband SIW-fed patch antenna array for 60 GHz band [30]. A single-layered SIW feeding network with wideband T-junctions and wideband high-gain cavity-backed patch antennas are employed to achieve high gain of upto 19.6 dBi in a 4×4 array with fractional bandwidth of 22.6% (53.7-67.4 GHz). The antenna has a multi-layered structure, which can be fabricated by conventional low-cost single-layered PCB technology and then realized by stacking and fixing all single layers together. Another study by T. Djerafi et al., demonstrate the state-of-the-art SIW techniques in design and realization of innovative, low-cost, low-profile and low-loss mm-wave antenna elements, feeding networks and arrays for various wireless applications [31]. The developed structures are based on two techniques: multilayer stacked structures and E-plane structures. Several antennas and antenna arrays such as Yagi-like array, integrated pyramidal horn antenna, patch antenna array and broadside rod antenna along with novel wideband feeding networks are discussed in this study. A 16-element 77-81 GHz phased-array receiver with $\pm 50^0$ beam scanning for advanced automotive radars is reported by B.H Ku [8]. The phased-array receiver is based on a single SiGe chip with RF beamforming capabilities, which is packages using low-cost bond-wire techniques and attached to a 16-element linear microstrip array. The antenna array has a directivity of 29.3 dB, a gain of 28.0 dBi at 77-81 GHz range and can scan $\pm 50^0$ in the azimuth plane in approximately 1^0 steps. The array is 38.5×38.5 mm^2 in size and its primary application is that of an imaging radar in automotive environment. The fabricated radar system is shown in Figure 15. A similar automotive radar transceiver operating at 77 GHz is reported by Infineon Technologies [14].

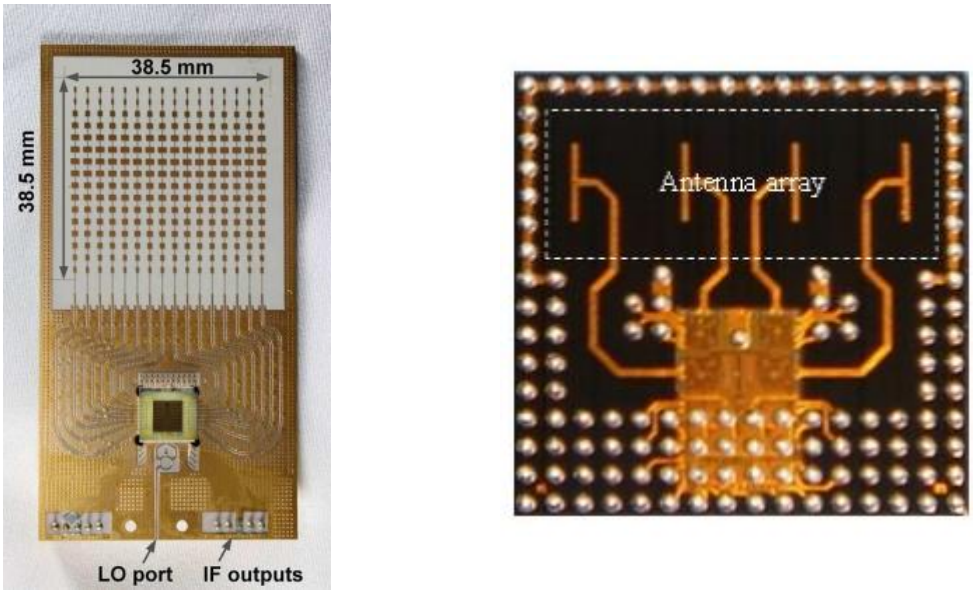


Figure 15: (a) 16-element phased antenna array with integrated DC control (b) Four channel transceiver with in package integrated antennas by Infineon Technologies.

Image Courtesy: (a) B.H. Ku et.al. UCSD (b) J. Bock, Infineon Technologies

2.6 Device-to-Package Interconnections

Interconnects serve as streets and highways of the IC, connecting external elements to the IC and interfacing it with the outside world. Interconnect design can vary depending upon the complexity of the IC. For 5G and mm-wave, interconnects need to be ultra-small, low-loss and should be cost effective to be commercialized in a fabrication process. Fabricating these intricate structures, interconnects and adjoining vias, is one of the most process-intensive and cost-sensitive portions of chip manufacturing. A few interconnect types are shown in Figure 16.

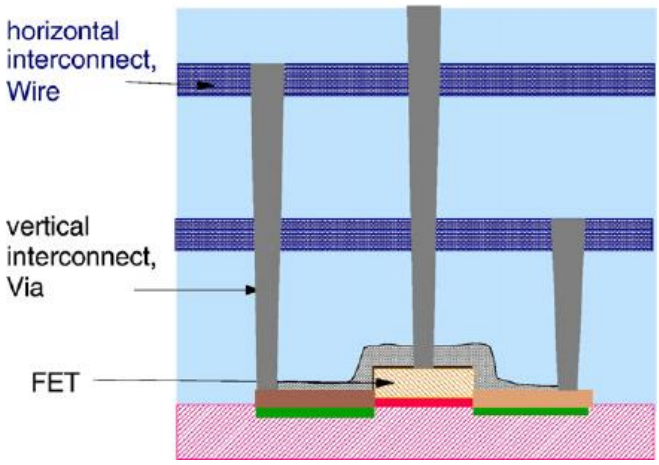


Figure 16: Major interconnect types.

Since the interconnect length is comparable to the wavelength of the operating system at mm-wave frequencies, loss becomes a serious concern. This concern drives the designers to opt for even shorter transmission distance to reduce the loss other than on PCB or cable-connected board. Interconnects from chip to antenna feeding line is demonstrated to have 0.7 dB loss in a study by C.H Tsai et. al. from TSMC [32]. This study revolves around integrating a 4×4 antenna array integrated with RF chip using integrated fan-out wafer level packaging (InFO-WLP) technology. The array operates in 57-64 GHz range with a 11.6% fractional bandwidth and boasts a gain of 14.7 dBi in a small form factor of 10 × 10 × 0.5 mm^3. Interconnect loss study is also performed using a 1600 μm long CPW transmission line. This loss is compared with chip pad to antenna port through C4 bump on LTCC substrate and though solder balls on LTCC substrates. In these cases, the loss is 1.6 dB and 4.9 dB, respectively, at 60 GHz. This can save 19% higher power amplifier output power compared with that of a flip-chip package. The insertion loss of these interconnect types is graphically shown in Figure 17.

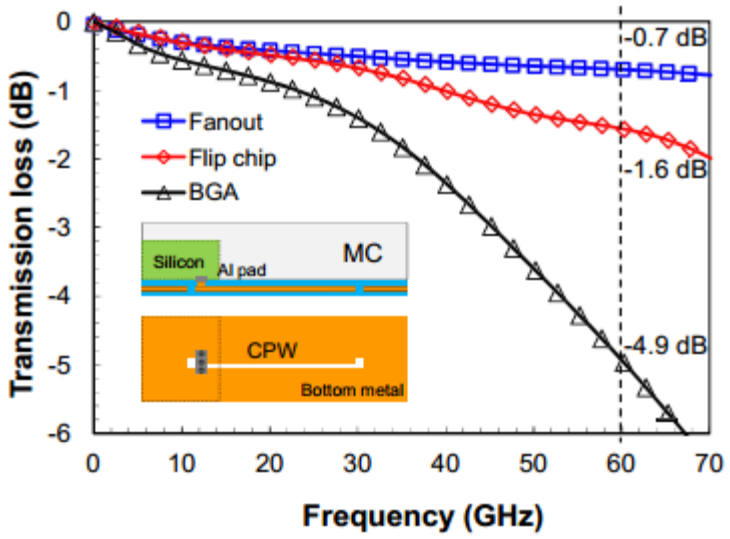


Figure 17: Transmission loss in fan-out, flip-chip and BGA interconnect structures.

Image Courtesy: C.H Tsai et. al. TSMC Ltd.

Various types of interconnect techniques are depicted in Figure 18. These techniques have evolved over time with the advancements in microelectronics. The most popular techniques for 5G applications are fan-out, ball-grid array (BGA) and their variants. Wire-bonding is a very popular technique for RF applications to connect a die to its lead-frame but it has

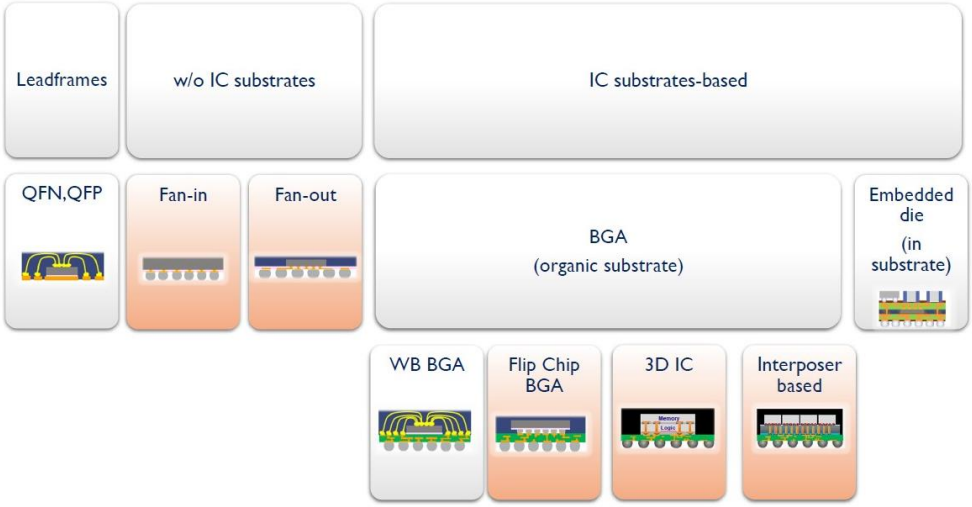


Figure 18: Types of fan-out packages.

several limitations at mm-wave frequencies, of which increased loss and higher coupling are the prominent ones. Fan-out and its variants have become popular in the recent years due to their substrate thinness, lowest parasitics, ease of fabrication, low cost, scalability for high integration level and greater number of interconnections. It provides a smaller package footprint with higher IOs along with improved thermal and electrical performance. It takes individual die and embeds them in a low-cost material such as epoxy mold compound with space allocated between each die for additional IOs, avoiding the use of relatively expensive real estate of the substrate.

2.7 Substrate Technologies

Substrate provides wiring or interconnections between various circuit elements. Various substrate technologies have evolved over time. These include ceramic, organic, silicon and glass, and are used for a variety of applications. This section will focus on three major substrate technologies: organic laminates, ceramic (LTCC) and glass. Their fundamentals and the reasons as to why they are used as substrates to house active and passive devices are discussed. Moreover, processing of each substrate technology will also be discussed in detail.

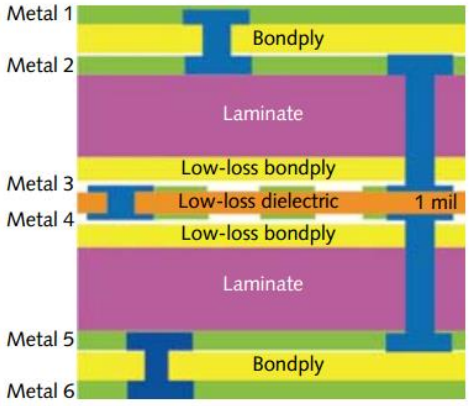


Figure 19: Cross-section of a typical MLO substrate.

2.7.1 Organic Laminates

Structure of an Organic Substrate

A typical multilayered organic substrate is shown in Figure 19. It consists of one or more RF dielectric layers embedded between layers of other laminates or buildup films to provide routing, shielding and bonding pads for SMT or SMD passives and RFIC die placement. Silica-filled hydrocarbon bondplys and buildup layers are used for the outer layers to provide rigidity, low moisture absorption and low z-axes CTE to help ensure reliability. Inner dielectric layers must have low loss at the operating frequency and should be thin enough to enable high capacitance densities and minimize total package height. High dielectric constant is preferred by the designers to achieve smaller circuit size and higher capacitance densities.

Epoxies have been the workhorse dielectrics for organic substrates. They offer excellent adhesion and easy processability thorough lamination and metallization. However, they suffer from their relatively higher loss tangent. Low-loss organics such as liquid crystalline polymers (LCP) or PTFE are emerging to address the concerns with loss tangent. PTFE composites developed with advanced filler materials are conventionally used to increase Dk without significantly increasing loss. This gives the options for either low or high dielectric constant in the inner layer and can be changed as per the requirement of the application. Standard multilayer or sequential lamination processing is used to complete package structure. The finished MLO substrate exhibits excellent RF performance because of low-loss dielectric materials used as both core and buildup [33].

Surface metallization in the outer layers is used as a barrier to form reliable solder joints. Copper is considered disadvantageous as a surface metal as it oxidizes quickly and reacts with solder to form a brittle intermetallic compound with undesired electrical and physical properties. A good example is nickel, which acts as an excellent barrier metal and is coated with ultra-thin gold to prevent bridging of adjacent solder joints. Some examples of surface metals are electroplated nickel along with matte tin, hard gold, soft gold and electroless plated nickel with immersion gold, hot-air solder leveling (HASL) and organic solderability preservative (OSP).

Fabrication of an Organic Substrate

There are three types of patterning processes in a typical organic substrate fabrication process: subtractive, semi-additive and fully-additive. The semi-additive process is most common process for patterning metal on buildup dielectric films whereas subtractive process is common in patterning metal on the laminate core material. A typical organic substrate fabrication process is shown in Figure 20.

Subtractive Process (Etching)

The subtractive process is performed to pattern the laminate core with metal. As the name implies, the process is the removal of undesired copper from the core. The core can be either plated with a standard thickness of copper as in case of many commercially available laminates or it can be plated during the process to achieve desired thickness. The process is shown in Figure 21.

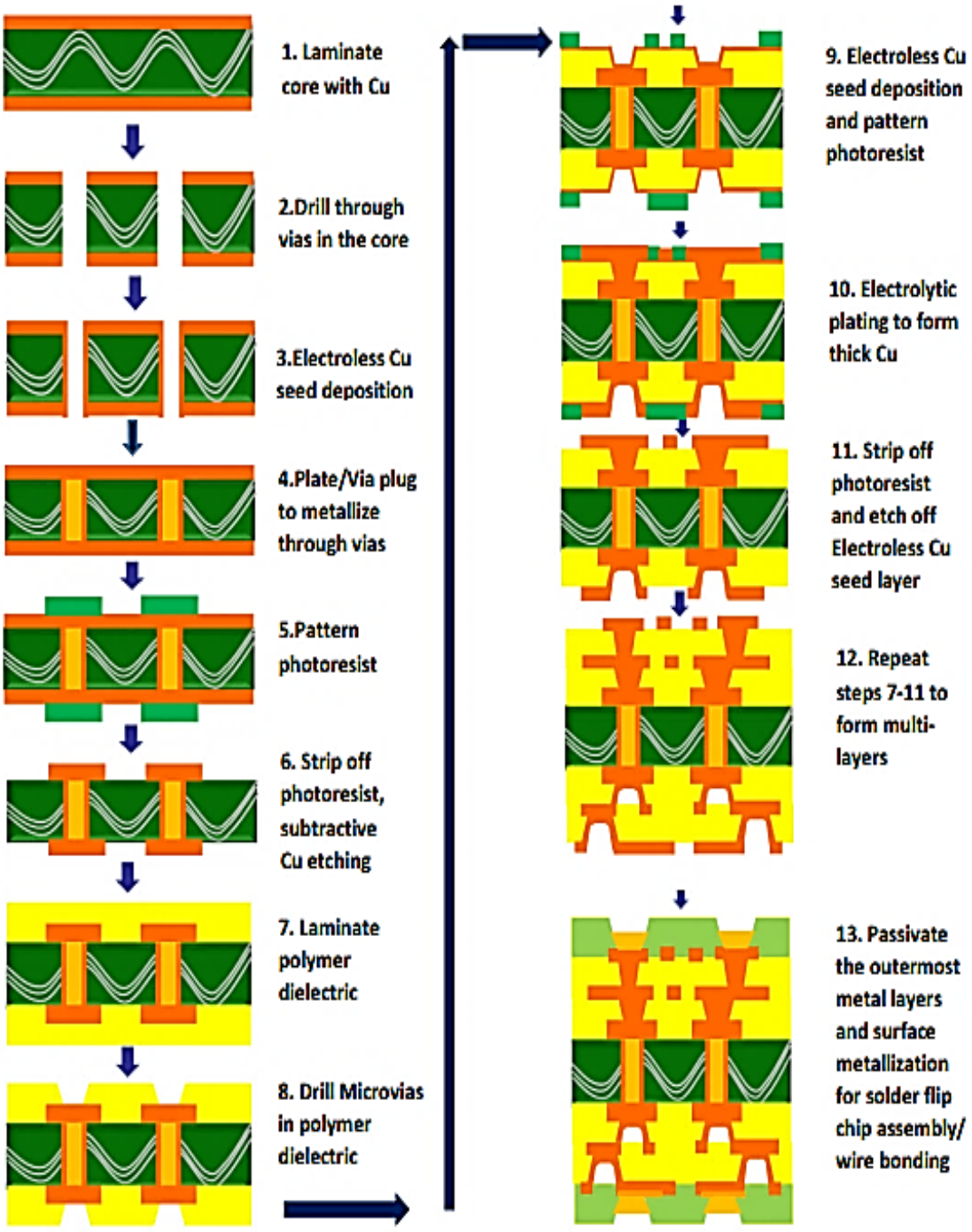


Figure 20: A typical process flow for fabrication of organic substrates.

Image Courtesy: Chandra Nair, Georgia Tech

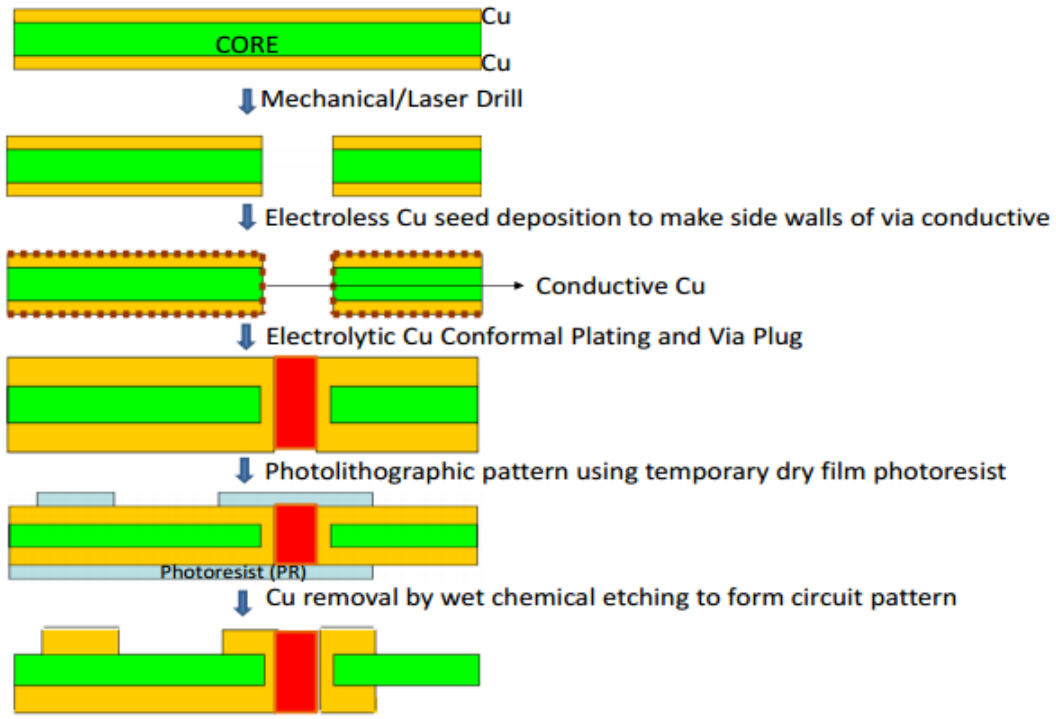


Figure 21: Formation of conductive patterns with through vias in a laminate core.

Image Courtesy: Chandra Nair, Georgia Tech

Semi-Additive Process (SAP)

The semi-additive process involves deposition of electroless copper seed layer followed by patterning the circuit using electrolytic plating and finally etching the seed layer from the undesired areas. For this reason, the process is termed as semi-additive as it is neither purely additive requiring no etching nor purely subtractive in which only etching of copper is performed. A step-by-step cross section of SAP is shown in Figure 22.

An important comparison is the feature size of core and buildup layers. The core metal patterns are used for power delivery networks which need to have wide and thick conductor for efficiency, hence the feature size of copper patterns on the core are not of a major concern. This makes the cheaper subtractive etching process ideal for processing the core laminate. However, the buildup layers or RDL require fine feature size since they are

interfacing the IC with the package using ultra-small interconnects. Moreover, IC bumps also require interfacing with the PWB so fine feature is an inherent requirement of buildup dielectric layers. The beauty of SAP appears in the fabricated lines. As shown in Figure 23, the lines are rectangular if fabricated using SAP in contrast to having a convex profile in the subtractive process for very small linespace.

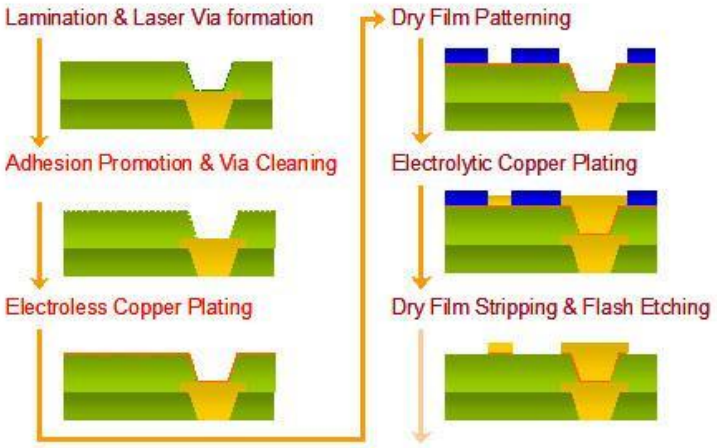
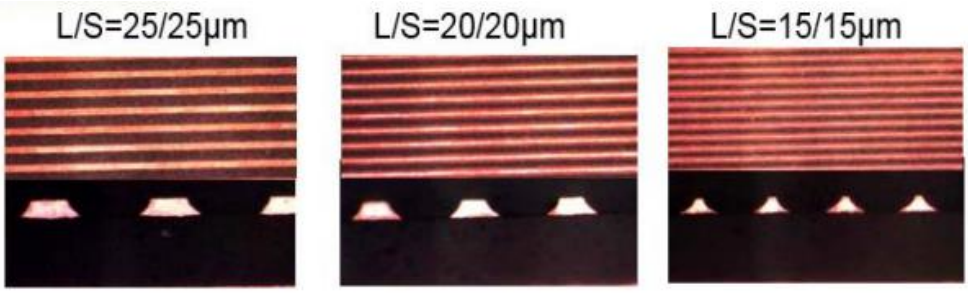


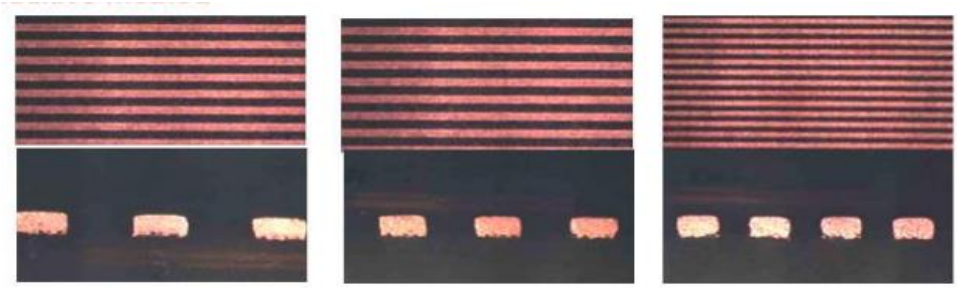
Figure 22: Patterning buildup layers using semi-additive process.

Lamination of Polymer Buildup Dielectric Film

After patterning the core, the next step if the lamination of polymer buildup dielectric film on the core. Usually, dry film polymer dielectrics are used and the process by which lamination is performed is known as vacuum hot press lamination. A hot step is included in the process to ensure that the dielectric is planarized.



(a)



(b)

Figure 23: Linespace profile (a) subtractive process (b) semi-additive process.

Image Courtesy: Dr. Venkatesh Sundaram, Georgia Tech

Microvia Formation

Vias are formed after the buildup film is laminated on the core. Laser drilling process is used to drill the microvias. They are termed as microvias because of their small diameter which can be as low as 30 μm. Different types of laser processes are summarized in Table 2. The absorption spectrum of a material must be considered before selecting a laser.

CO_2 lasers emit infrared light with wavelength range of 9.3-10.6 μm. CO_2 lasers vaporize the buildup layer polymer in case of epoxies and glass filled dielectrics by photo-thermal ablation in which high-energy infrared photons break the molecular bonds through excitation. These lasers can be used to drill vias at very high speeds, high throughput and the whole process is inexpensive in nature. However, relatively long wavelength limits the

minimum focus diameter in each working field area so it is not used to drill vias below 45 µm diameter. To drill vias in the range lower than 45 µm in the range of 20-50 µm, UV lasers are used as they operate at 355 nm wavelength. The mechanism of UV laser ablation

Table 2: Laser Technologies for Microvia Drilling.

CO_2 Laser	UV, YAG Laser	Excimer Laser
• Thermal Process	• Chemical/Thermal Process	• Mostly chemical process
• Point-to-point drilling	• Point-to-point drilling	• Mass via generation-projection lithography
• High throughput, inexpensive	• Medium throughput, high cost	• Potential for very high throughput, scalable, high cost

is based on a combination of photo-thermal and photo-chemical ablation. These beams can effectively break the molecular bonds and ablate most of the dielectric polymers used in substrate packaging. Copper has absorption at UV wavelengths so it is critical to stop at the copper pad to prevent damage to it. The beam of UV laser can be focused at a small spot with high power density to precisely drill small vias but it is expensive as compared to CO_2 laser. Excimer lasers can drill even smaller vias than UV lasers since the wavelength used in these lasers is 248 nm but they are even more expensive than UV lasers. Excimer lasers are in research phase as of now and they will be made commercial once the operation costs go down.

Other via formation technologies such as photo-via and plasma etching are also used to a small extent. The low-cost process of photo-via requires layers of photo-imageable or photosensitive permanent dielectric materials. These photosensitized polymers work like photoresists and are available in many chemistries such as polyimide, benzo-cyclobutene (BCB) or epoxy. They are exposed through a chrome mask to form the vias. Finally, the exposed and developed films are cured to obtain the final cross-link properties of that polymer.

2.7.2 Ceramic Substrates

Ceramics are defined as inorganic and nonmetallic solids made of compound metals (aluminum, zirconium, titanium, tungsten etc.) and nonmetals (oxygen, nitrogen, carbon, fluorine etc.). Oxides, carbides and nitrides such as aluminum oxide, silicon carbide and aluminum nitride have special properties such as thermal conductivity and low CTE to meet substrate requirements. The major focus of this subsection will be cofired ceramics and specifically, low temperature cofired ceramics or LTCC. Cofired ceramic devices are monolithic, ceramic microelectronic devices where all the layers of the device, whether they are conductive, resistive or dielectric materials, are fired together at the same time in a kiln or an oven. The technology is used commonly in multilayer packaging electronics industry. Cofired ceramics are made by processing several layers of the device independently and in the final step, they are assembled together into a device. This is different from the processes used in silicon industry where the process advances serially. Cofiring is generally divided into two categories based on temperature: low temperature means that the sintering temperature is below 1000^0C whereas high temperature is around 1600^0C.

Ceramics are a very established technology and they have been used for substrate applications for decades now. It is because of the combination of the properties discussed below.

- **Low loss tangent:** Ceramics have low loss tangent at microwave frequencies which makes them an ideal candidate for RF applications which require high Q passive devices
- **High melting point:** Ceramics have a very high melting point which makes then thermally stable during processes such as thin and thick-film wiring formation and solder assembly.
- **High modulus of elasticity:** Substrate flatness is a very critical parameter for building high-density multilayer wiring on the ceramic substrate and for flip-chip assembly. Ceramics have high modulus of elasticity which mitigates the warpage during sintering process. Mitigation of warpage helps in relaxing the design rules for the circuit and package itself
- **High Insulation Strength:** Ceramics maintain a high insulation strength even after the application of high voltage on surface conductors
- **Low CTE:** Glass and ceramics are the best materials to match CTE. Ceramics are mostly suitable in the CTE range of 3-7 ppm/K for substrate applications. They have excellent CTE match to silicon, GaAs, SiGe, SiC and GaN devices which leads to enhanced interconnection reliability
- **High electrical resistivity:** This characteristic of ceramic ensures minimum power leakage to adjacent conductors in case of high power applications

- **Immune to moisture absorption:** Ceramics are generally hermetic which means that they have no affinity to gases and moisture, which helps in preventing corrosion and electro-migration related failures

Structure of a Ceramic (LTCC) Substrate

A typical LTCC stackup is shown in Figure 24. It has multilayered wiring comprising of conducting traces and vias separated by thick ceramic dielectric layers. A ceramic package has five elements:

1. **Dielectrics:** Each layer in a ceramic is composed of a dielectric. Ideally, all the dielectrics are CTE matched
2. **Conductors:** Conductors such as copper are used for signal transmission and distribution between different layers and components in the package. They are also used in the inner layers to embed passives such as resistors and capacitors
3. **Metal Caps:** They are brazed on top or bottom of chip depending on its location in the package to protect it and ensure high reliability
4. **Pin Grid Array:** Ball or pin grid arrays are used to interface the package to the board
5. **Precision Structures:** Precision microwave transmission lines and embedded passives within the substrate are used to support variety of functions.

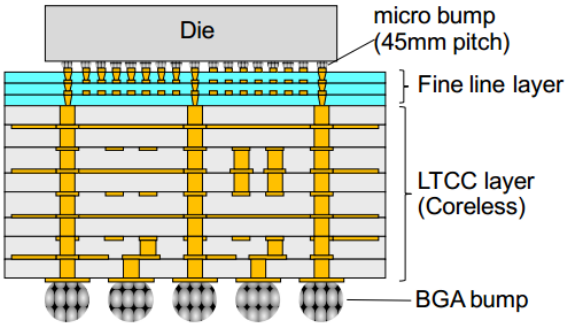


Figure 24: A typical LTCC stackup.

Alumina has been very popular for ceramic packages since 1980s because of its dielectric properties of low loss, high dielectric strength, resistance to electromigration and low cost. But it posed two problems: it needs to be processed at high temperatures which makes it incompatible with several metals and it has high CTE which affects the interconnection reliability. These problems are solved by adding glass to ceramics. A suitable glass-based composition that can be sintered at low temperatures and then can be partially or completely crystallized to ceramics with high mechanical strength is the best solution. These materials are often termed as glass-ceramics. They typically consist of glass-forming compounds mixed with alumina or silica. A few examples of glass-ceramics are oxide mixtures of silica and alumina, combined with oxides of barium, magnesium and calcium.

Alumino-silicates of lithium and boron, which can form as high as 40 volume percent of the total dielectric material, are typically added to alumina. This results in lowering the sintering temperature to 850^0C. The glass phase melts at low temperature, completely wetting the alumina and aid in sintering. In the final material, both glass and ceramic phases coexist and possess valuable properties of both crystals and glasses. These are referred to as glass plus ceramics. Glass-ceramics and glass plus ceramics are used in LTCC

technology. They offer rugged, hermetic and reliable packaging with the ability to have multiple layers and high wiring density along with reduction in z and x-y directions. Thermal conductivity is one of the important parameters to take care of in the high-performance packaging as heat goes through the ceramic itself for dissipation unlike the flip-chip package, in which heat can dissipate through the back of the die.

Fabrication of Ceramic Substrates

The fabrication of ceramic substrate can be divided into two major categories:

- Single-chip packages
- Multi-chip packages

Conductor wires are screen-printed on the top of substrate to form metal traces and contact pads. Metallization of green-sheet is also accomplished by extruding the metal paste through a mask in contact with the sheet. This process is also used to fill vias. Multilayered ceramic fabrication allows for parallel processing of many single sheet ceramics, making it possible to obtain high yield. The process is shown in Figure 25. The sintering temperature of the ceramic powder must be less than that of the melting temperature of the metal used as conductor. Therefore, it dictates the metal wiring used for the circuitry.

Atomic movements become significant at temperatures approaching 70 percent of melting temperature of the metal and generally, sintering is performed at this temperature. For alumina, this temperature exceeds the melting point of copper. Therefore, tungsten or palladium are used for wiring. Formation of liquid phase expedites the sintering process and lowers its temperature, making it compatible with copper wiring.

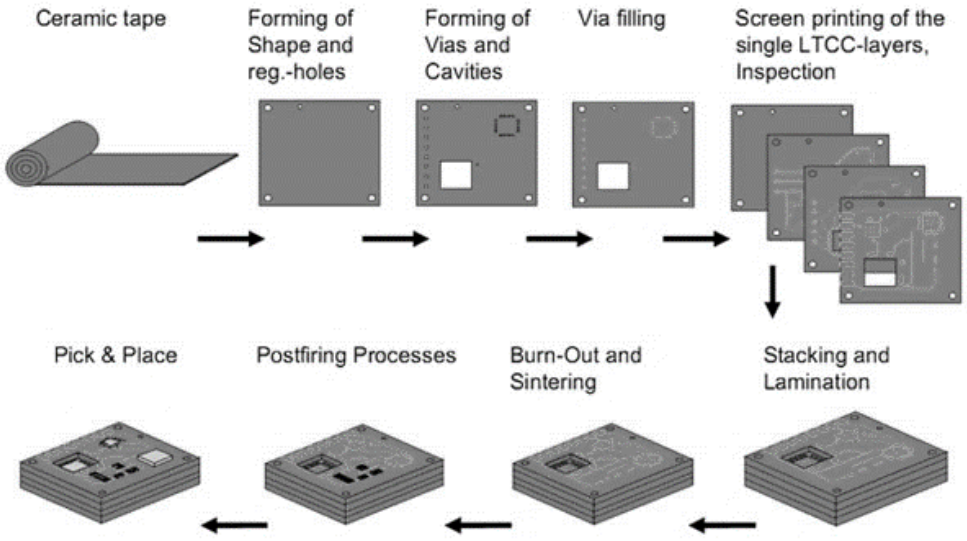


Figure 25: Fabrication process of LTCC.

Consequently, this led to development of LTCC with glass-ceramic or glass plus ceramic. For example, $MgO\text{-}SiO_2\text{-}Al_2O_3$, a glass-ceramic with low Dk, CTE match to silicon and steep viscosity-temperature relation for easy binder burn-off is a common LTCC material.

Hermetic Sealing

For environmental, chemical and mechanical protection of the chip, a metal cap is glued over the chip. Metal glues based on solder or braze are widely used because of their low melting point and hermeticity.

Package-to-Board Interconnections

High aspect ratio metal pins, known as pin grid array (PGA), are used to connect large glass-ceramic modules of same CTE as silicon to the system board. Copper connector pins are swaged into the holes of the substrate and entire structure is immersed in a solder bath to form contacts between the pins and the metal traces. Higher aspect ratio pins accommodate for the large CTE mismatch between low-CTE packages and boards. On the

other hand, the interconnection pitch of PGAs has not scaled below 1 mm which limits their application in today's applications.

2.7.3 Glass

The term "glass" refers to solids that possesses a non-crystalline or amorphous structure and exhibits a glass transition temperature when heated. The most common types of glass are silicate glasses based on silica (silicon dioxide or quartz), which is the primary constituent of sand.

Glass has several useful electrical properties which makes it suitable for substrate applications [34]. Some of them are discussed below.

- **Stable Dk and Df:** Glass has stable Dk and Df for a wide range of frequencies. Research conducted in Georgia Tech PRC by Jialing Tong showed less than 10% variation in Dk upto 50 GHz for Corning SGW 3 glass, as shown in Figure 26. The Df ranged from 0.006 to 0.011 in the whole frequency range

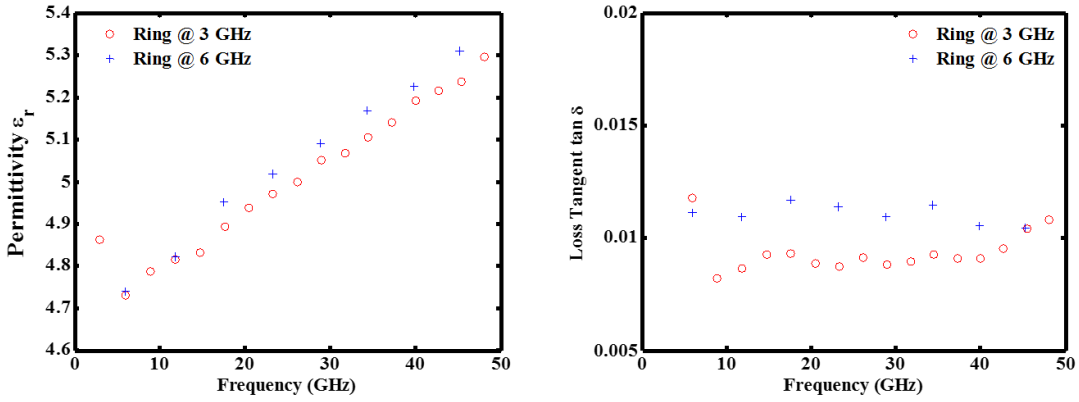


Figure 26: Glass characterization at Georgia Tech PRC.

Image Courtesy: J. Tong et. al Georgia Tech

- **Dimensional Stability and high reliability:** Glass exhibits excellent dimensional stability, which makes it an attractive choice for processing high-density interconnects. Smaller features can be easily manufactured on glass with high reliability due to its superior dimensional stability
- **High electrical insulation:** This property ensures that closely-spaced conductors will have stable electrical isolation among them despite the application of higher voltage
- **High-temperature stability:** Glass can be processed at high temperatures without any change in physical properties if the temperature is less than the glass transition temperature. Within that temperature, the electrical properties are fairly stable
- **Low CTE:** Glass has low CTE that can be conveniently matched to that of Si and other active devices.
- **Low Thickness:** Glass is available in a wide range of thicknesses such as 100, 150, 200 and 300 µm. This can effectively constrain the package height.
- **Low Surface Roughness:** Glass has almost zero surface roughness at higher frequencies, which makes it an ideal candidate as a core material. This property makes it suitable for mm-wave applications. Multiple redistribution layers (RDL) can be stacked on glass for a compact, low loss and superior-grade packages.

Glass is used as a core material inside the packages. Buildup materials are stacked onto it and metallized with copper traces to form the wiring layers. Active components are assembled onto either sides of the glass substrate. An alternative emerging technology is to use glass as the fan-out package, where chips are assembled into the cavities that are pre-formed in glass. The assembled substrate is planarized and build-up layers are formed

onto the active side of the IC, with microvias directly connecting them to the IC pads. Glass substrate offers several benefits such as reduced die shift from its dimensional stability, silicon-like precise RDLs, board-level reliability, and ultra-low loss. The package can also support embedded passives, multiple ICs and antennas along with BGA interfaces to connect to PWB. The line widths can be as low as 2 µm to meet the emerging RDL needs. The benefits of Georgia Tech glass fan-out (GFO) approach is shown in Figure 27.

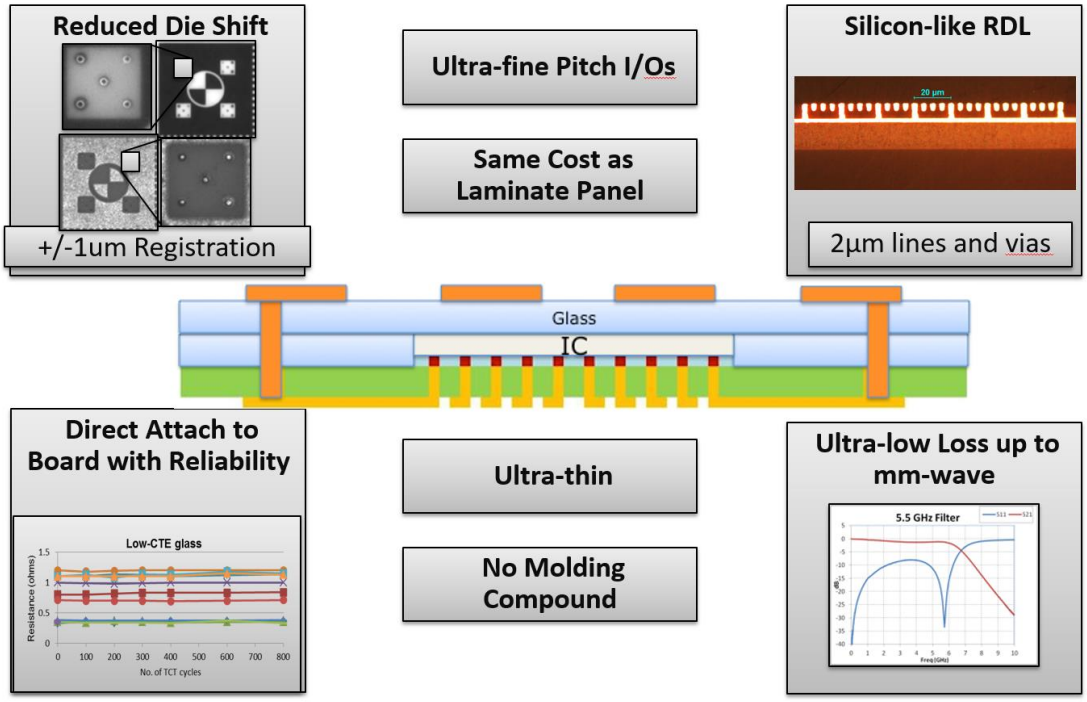


Figure 27: Georgia Tech glass fan-out (GFO).

Image courtesy: Dr. Venkatesh Sundaram, Georgia Tech

2.8 Summary

In this chapter, the basic elements of 5G systems – ICs, transmission lines, passives, antenna, and interconnects are reviewed. Major R&D advances in the areas of passives and

antennas are highlighted. Fundamentals of transmission lines and their selection criteria are also briefly discussed. The last part of the chapter discusses three substrate technologies in detail: organic laminates, ceramics (LTCC) and glass. The properties that make these candidates suitable for 5G substrates are described. The substrate structure and processing is explained for each of these candidates. The superiority of glass over laminates and ceramics is illustrated.

CHAPTER 3

SUBSTRATES FOR 5G APPLICATIONS

The objective of this task is to explore, model, design, fabricate and characterize next-generation 5G substrates that can attain superior electrical performance metrics such as transmission line loss of less than 0.05dB/mm, interconnection parasitics of less than 50 pH, via transition loss less than 0.02 dB, and low overall antenna-to-IC parasitics for antenna-integrated packages. The main focus is to: a) evaluate various substrate technologies for 5G applications and identify the ideal candidates, b) simulate and compare the performance of transmission lines with 5G substrate candidates such as low-loss laminates and glass, c) fabricate and characterize the performance of glass substrate technologies for 5G applications. Substrate properties and criteria that affect the electrical performance and processability to achieve target metrics are discussed at first, and then applied to several candidate substrates, in order to evaluate their effectiveness in reaching the performance metrics. Three major substrate technologies are discussed:

1. Organic Laminates
2. Low Temperature Co-fired Ceramics (LTCC)
3. Glass

These substrate technologies are compared against each other and their merits and demerits are discussed. Traditional and emerging organic laminate substrates are considered. The first part of the chapter discusses substrate candidates in two major categories: core and buildup layers. The second part of the chapter describes the design, fabrication and

characterization of test vehicles with standard transmission lines in order to assess the viability of the substrate under test.

This chapter is organized as follows. The first section discusses the substrate properties for 5G applications. Various candidate materials and their properties are compiled and evaluated next. Modeling of transmission lines, test vehicle design, fabrication and characterization are discussed in the last section of this chapter.

3.1 5G substrate Selection – Key Attributes

To compare various substrate technologies, a set of parameters was created as a guide. Each substrate technology is compared against the same set of parameters in order to filter out their merits and demerits vs. each parameter. The parameters are discussed below with an ideal 5G substrate system in view:

3.1.1 Electrical Properties vs. Frequency

Dielectric Constant (Dk)

Dk consistency is critical as variation in Dk can result in impedance change of the transmission line and it can lead to dramatic variance in the desired results. Also, stability of this parameter with temperature and humidity is very important as it directly translates to loss due to the material itself. Lower Dk values reduce the field strength in the substrate and therefore helps in reducing the total loss. However, it makes the circuit physically larger as compared to a higher Dk material. On the higher hand, higher Dk values can reduce the circuit size at the expense of increased dielectric loss and fields are mostly concentrated in the substrate. At higher frequencies, usually fine features are required due

to reduction in wavelength and naturally that brings forward the requirement of low Df values which translate into lower loss for circuits.

Loss Tangent (Df)

Loss tangent or dielectric loss directly translates to insertion losses or degradation in Q factor. Therefore, it is the most important property. It is also important to note that the loss tangent is frequency-sensitive. Its stability with frequency will ensure that loss does not increase at higher frequencies. Ideally, it should be constant over the whole frequency band of operation.

3.1.2 Stability of Electrical and Physical Properties against Temperature and Humidity Variation

Substrates for 5G applications are required to have stable electrical and physical properties over a wide range of frequencies. This is an inherent requirement for sensor devices and networks which are exposed to harsh environments with varying temperature and humidity. This property will ensure the reliability of the system under a variety of external conditions.

3.1.3 Design Rule Capability

With more device integration and functionality, smaller feature size is a requirement inherent in modern systems. The substrate technology for 5G should be able to reliably handle ultra-small linewidths and line spaces. Moreover, the substrate system should be scalable in terms of design rules such as line/space, via size, core and RDL via diameter, core and RDL via pitch, IO density etc. for various applications.

3.1.4 Process tolerances

An ideal 5G substrate system will enable precise conductor and dielectric geometries, desired and controlled surface roughness, and minimal deviation in geometries and properties during processing and operation. Precise lithography patterning, dimensional stability during thermal processing, uniform plating and deposition rates are the key attributes for process tolerance. Substrates are exposed to a variety of chemicals and temperature variation during the fabrication process. This can sometime lead to changes in physical and electrical properties of a substrate. For example, plating and etching are processes that can change the surface roughness of the material. Moreover, CTE match with buildup dielectrics is also important to minimize substrate warpage and stresses.

3.1.5 Multilayer Capability

Layer count is a very important aspect of substrate technology. Layer count directly translates to the ability to handle complex design requirements with high I/O count for 5G applications. An ideal 5G substrate system should be able to handle multiple layers with minimum interface roughness, loss and high reliability.

3.1.6 Panel Size, Process Throughput and Cost

Panel size is a very important aspect of a substrate technology. Large-area panel processing directly results in more throughput and lower cost per unit produced. Process throughput also influences how fast the panels can be processed with maximum efficiency, and directly impacts the cost. Deposition or plating rate, number of vias drilled per second, large dry-film processing etc. are the key attributes for high throughput. Processing in large area, using high throughput processes, lowering the material as well as process cost, and

simultaneously increasing the yield are desired qualities for any high-volume manufacturing.

3.1.7 Manufacturing Supply Chain Readiness

Finally, a substrate system with all the ideal properties should not be just confined to research, but eventually available from substrate manufacturing giants to make it mainstream and accessible for high-volume applications.

3.2 Candidates for 5G Substrates

An extensive paper study was performed to filter out the best candidates for the materials for each substrate technology. The presented materials are divided into two major categories: Core and RDL. The list contains both commercial and advanced research materials that are yet to enter market. The materials are compared in terms of their electrical properties and keeping in mind the ease of in-house process development along with their processability with a variety of common processes and buildup materials used in semi-additive processing.

3.2.1 Core Materials

The core materials are divided into three major types:

- Glass (Table 3)
- LTCC (Table 4)
- Organic Laminates (Table 5)

The options for each material along with their electrical properties such as dielectric constant and loss tangent are given in the following tables:

Table 3: Glass Core: Materials and Properties.

Glass	Dielectric Constant	Loss Tangent
Corning SGW 3 (Low CTE alkali-free)	5.15 @ 10 GHz	0.007 @ 10 GHz
Corning SGW8.5 (High CTE with alkali)	6.9 @ 1 GHz	0.023 @ 10 GHz
AGC EN-A1	4.9 @ 10 GHz	0.0056 @ 10 GHz
Schott AF-32 eco	5.1 @ 5 GHz	0.0049 @ 5 GHz
Schott MEMpax	4.4 @ 5 GHz	0.0073 @ 5 GHz
Asahi Glass low loss	5.41 @ 35 GHz	0.0090 @ 35 GHz

Table 4: LTCC Core: Material and Properties.

LTCC	Dielectric Constant	Loss Tangent	Operating Frequency	Conductor
Dupont 9K7	7.1 ±0.2	0.001	Upto 100 GHz	Silver, Copper
Ferro A6-S	5.9±0.2	0.001	Upto 100 GHz	Silver
DP943	7.4	0.002	Upto 40 GHz	Silver
DP951	7.8	0.014	Upto 40 GHz	Silver
NGK-NTK NOC-F1	6.0	0.0021	Upto 60 GHz	Copper
Hitachi Metals LTCC*	8.13	0.00086	Up to 14 GHz	Silver
TDK-Epcos*	-	Low Loss	-	Copper

Table 5: Laminate Core: Materials and Properties.

Material	Dk				Df			
	10 GHz	28 GHz	38 GHz	45 GHz	10 GHz	28 GHz	38 GHz	45 GHz
MGC BT Laminate	3.350	3.400	3.400	3.400	0.0040	0.0040	0.0041	0.0043
Panasonic Megtron 7	3.600	3.600	3.600	3.600	0.0040	0.0040	0.0040	0.0050
Rogers RO4350B	3.730	3.715	3.710	3.700	0.0037	0.0039	0.0039	0.0040
Rogers RO 4350B LoPro	3.640	3.630	3.620	3.600	0.0037	0.0039	0.0039	0.0040
Rogers RO4003C	3.650	3.640	3.635	3.630	0.0027	0.0028	0.0028	0.0029
Rogers RO4003C LoPro	3.525	3.520	3.520	3.510	0.0027	0.0028	0.0028	0.0029
Rogers RO4725JXR	2.55	-	-	-	0.0026	-	-	-
Rogers RO4730G3	3.0	-	-	-	0.0027	-	-	-
MGC HL972LF (LD)	3.4	3.4	3.4	3.37	0.004	0.004	0.004	0.004
Hitachi LW900G	3.6	-	-	-	0.0044	-	-	-
Hitachi LW910G	3.3	-	-	-	0.003	-	-	-
Panasonic R-G545 (R&D)	3.65	-	-	-	0.004	-	-	-
Panasonic R-G545 Low Loss (R&D)	3.4	-	-	-	0.003	-	-	-

3.2.2 Buildup or RDL Materials

The buildup materials are divided into two major categories: Prepregs and Buildup films. A prepreg is a fibrous material pre-impregnated with a synthetic resin. They are often used in making reinforced plastics and are very common in industry as buildup dielectrics. The dielectrics in both categories along with their electrical properties are summarized in Table 6 and Table 7 respectively.

Table 6: Buildup Materials: Prepregs.

Material	Dk				Df			
	10 GHz	28 GHz	38 GHz	45 GHz	10 GHz	28 GHz	38 GHz	45 GHz
Panasonic Prepeg R-5670(K)	3.220	3.220	3.220	3.220	0.0050	0.0050	0.0050	0.0060
Panasonic Prepeg R-5680 Low-Dk Glass	3.110	3.110	3.110	3.110	0.0020	0.0020	0.0020	0.0030
Panasonic R-G540	3.65	-	-	-	0.004	-	-	-
Panasonic R-G540 Low Loss	3.4	-	-	-	0.003	-	-	-
Rogers RO4450F Prepreg	3.52	-	-	-	0.004	-	-	-
Hitachi LW900G Prepreg	3.2	-	-	-	0.004	-	-	-
Hitachi LW910G Prepreg	3.1	-	-	-	0.0025	-	-	-
Hitachi HS100 Prepreg	3.4	-	-	-	0.0045	-	-	-
Hitachi HS100(E) Prepreg	3.2	-	-	-	0.003	-	-	-
Hitachi GWA900G	3.37	-	-	-	0.0024	-	-	-

Table 7: Buildup Materials: Films.

Material	Dk				Df			
	10 GHz	28 GHz	38 GHz	45 GHz	10 GHz	28 GHz	38 GHz	45 GHz
Rogers 2929	2.940	2.940	2.940	2.940	0.0030	0.0030	0.0031	0.0031
ABF GY-11	3.200	3.200	3.200	3.200	0.0042	0.0043	0.0043	0.0044
Hitachi Chemical AS-500S	3.500	3.500	3.500	3.500	0.0030	0.0030	0.0031	0.0032
Dow 14-P005 BCB Dry Film[1]	2.65	-	-	-	0.0015	-	-	-
New ABF Low Loss Film2	3.2	3.2	3.2	3.2	0.0042	0.0043	0.0043	0.0044
JSR New Low Loss Polymer	2.46 – 2.67	-	-	-	0.0027 – 0.008	-	-	-
Rogers XP	2.6	2.6	2.6	2.6	0.0023	-	-	Expect to be flat

3.3 Comparison of Substrate Design Rules

The design rules for the three substrate technologies are compared against each other. The parameters that will be discussed are panel size, core via diameter and pitch, RDL line width and line space, line width tolerance, RDL via diameter and layer count. Each of the substrate technologies have their strengths and weaknesses. The design rule summary for these candidates is given in Table 8.

Table 8: Design Rule Summary.

Material	Panel Size (R&D, Mfg.)	Core Via Dia.	Core Via Pitch	RDL L/S	LW Tolerance	RDL Via Dia.	Layer Count
Laminates (PWB)	510mm x 510mm (IC Sub) 900mm x 1200mm (PWB)	40 µm	>100 µm	30/30 standard 15/15 advanced	10-20%	N/A	High (>10)
RDL on Laminate		-	-	8/8 standard 2/2 µm advanced	-	30µm standard 10 µm advanced	Up to 6 each side typical
LTCC Core	200 x 200 mm Standard 300mm x 300mm Limited Availability	60 µm Typ.	120 µm Typ.	50/50 standard 30/30 advanced	<5%	-	High (4-20)
RDL on LTCC		-	-	2/2 µm	TBD	10 µm/ 20µm pitch	3 (top side only)
Glass	150mm x 150mm (GT Now) 300mm x 300mm (GT by Summer 2017) 510 mm x 510 mm (Mfg)	25 µm (R&D)	50 µm (R&D)	2/2 µm	±2% (Target)	5 µm/ 20 µm pitch	6-8 (double side)

As it is evident from the table, line/space of 2 μm can be achieved on glass and RDL layers with very strict tolerance of ±2%. Other substrate technologies fall short in this case. Panel size also plays a major role in the processing cost of package substrates. Although laminates have large panel size, they fall short in via diameters and linespace domain due to low tolerance. LTCC have small panel sizes which makes it very costly compared to other technologies. These materials are compared in Table 9 in terms of their electrical and physical properties. A more meaningful comparison involving another set of parameters is summarized in Table 10.

- **Multilayer Capability in Core** – Ceramic is best, laminate is second, Glass does not have multilayer core capability
- **Dielectric Loss –** Ceramic is best, laminate has limited low loss availability, glass has low-loss options emerging
- **Conductor Processing Capability** – Ceramic has the worst core conductor processing capability, laminate is better, while glass provides the best conductor processing (glass is better than laminates due to smooth surface, while ceramics requires polishing)
- **Surface Roughness** – Glass has least surface roughness to suppress high-frequency conductor losses, followed by laminates and ceramic
- **Thinness** – Glass has best potential for scaling. Thin laminates are available but warpage is a bigger concern, while ceramics are most difficult to reduce thickness
- **Panel Size** – Laminate and glass have better potential for larger panel size (510 mm x 510 mm in substrate and >900mm in PWB), while ceramic has availability from some suppliers at 300mm x 300mm

Table 9: Comparison of the properties of substrate core materials.

Characteristic	Glass	Silicon	Ceramic	LCP	FR4
Dielectric constant (ε_r)	5-7	11.7	6-9	2.9-3.2	4
Loss tangent (tanδ @ GHz)	0.006 @ 10	0.015 @ 10	0.0012 @ 10	0.004 @ 60	0.025 @ 10
Coefficient of thermal expansion - CTE (ppm/K)	3-8.5	3	5.5-7.2	17	17
Surface roughness (nm)	<1	0.15-0.3	177	400-600	300-5800
Water absorption	0	0	0	0.040 %	0.1%-0.25%
Dimensional stability - Young's Modulus (GPa)	50-90	130-185	90-150	10-40	21-24

Table 10: Comparison of the processability of substrate candidates.

Material/ Properties	Multilayer Capability in Core	Dielectric Loss	Conductor Processing Capability	Surface Roughness	Thickness	Panel Size
Glass						
Organic Laminates						
Ceramic						

Glass presents itself as a promising material for interposers especially for high-speed and high frequency applications such as 5G.

3.4 Recommendation for 5G substrate Candidates

After an extensive paper study in this research, 18 combinations of various substrates and build-up dielectrics were decided as feasible choices. These choices were boiled down to 3 combinations, which were the focus in modeling, design and fabrication. The choices are detailed below:

3.4.1 Low-loss RDL on Laminates

- Core: Rogers RO4725JXR and RO4830
- RDL: Rogers XP film, ABF GY-11/GL-102

3.4.2 Low-loss RDL on Glass

Core: Standard 100 μm AGC glass with loss tangent of 0.005 at 10 GHz

RDL: Rogers XP film, ABF GY-11/GL-102

3.4.3 Low-loss RDL on Ceramic

- Low-loss Cu-Polymer RDL on TDK-Epcos LTCC
- RDL: Same material options as Laminate and Glass

Rationale for Choosing Rogers RO4725JXR and RO4830

- Low Dk and Df at 37 GHz and 127μm thickness
- Stability of electrical properties at higher frequencies
- Easier Processability

Initially, two sets of laminates were chosen as discussed above. However, RO4725JXR was not available with the target thickness of around a 100 μm. Therefore, the focus shifted to RO4830 by Rogers. For glass test vehicle, AGC glass of 100 μm thickness was used.

3.5 Modeling, Fabrication and Characterization of Transmission Lines

The objective of this sub-task is to demonstrate transmission line (TL) structures with a loss of 0.05 dB/mm on various candidate substrates. The lines were designed with three sets of lengths with the following nomenclature for discussion:

- Full-Length CBCPW: 1.86 mm
- Half-Length CBCPW: 0.9 mm
- Quarter-Length CBCPW: 0.42 mm

Insertion Loss

Insertion loss of a component is the loss of signal strength or power when it is inserted into a system. It is usually expressed in relative units: decibels (dB) or absolute units: dB power relative to 1 mW (dBm), dB power relative to 1 µW (dBµ). Mathematically, it is defined as:

$$IL\ (dB) = -20 \log S_{21}$$

where S_{21} is defined as the s-parameter with ratio of reflected power from Port 2 to incident power from Port 1 given that Port 1 is terminated at the characteristic impedance of the system for a two-port network.

The significance of material properties can be illustrated through an analysis of various contributions to insertion loss. The free-space wavelength is 10.71 mm and 7.69 mm for 28 and 39 GHz respectively. Insertion loss has following components:

- *Dielectric loss* comes due to the material's electrical properties

- *Conductor loss* comes from non-ideal conductivity or finite resistance and from surface roughness.
- *Radiation loss* is mainly dependent on the design structure and conditions. Stripline circuits exhibit no radiation loss whereas microstrip and coplanar waveguide (CPW) circuits are prone to radiation loss at mm-wave frequencies. The materials with higher Dk values generally exhibit less radiation loss as compared to materials with lower Dk because electric flux is mainly concentrated inside the material itself. However, higher Dk translates to thinner conductor lines as compared to lower Dk for the same impedance, and consequently, more conductor loss is observed
- *Launching loss* occurs due to mode mismatches in launching the signal from a connector operating in TE mode and transmission line operating in quasi-TEM or TEM mode. This mismatch can cause radiation losses.

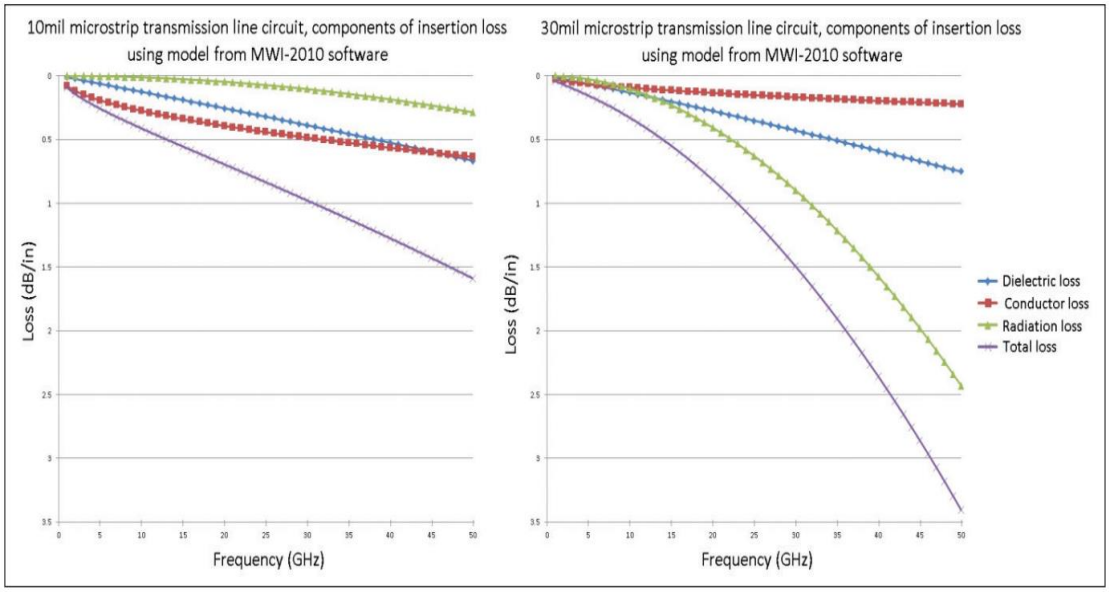


Figure 28: Insertion loss and its components.

Image Courtesy: Rogers Corp.

These components are depicted in a microstrip simulation model by Rogers Corp. in Figure 28. As evident from the figure, the components of the loss are dependent of the substrate choice as well as the design. For example, radiation loss can be minimized if the line lengths are adjusted to mitigate standing waves. Conductor loss remains mostly constant but it can be improved if the surface roughness is made as low as possible. Surface roughness is directly proportional to frequency which translates to higher contribution in insertion loss in mm-wave applications.

3.5.1 Modeling of Transmission Line Structures

The transmission line structures were modeled with the exact same specifications as that of the glass TV used in the fabrication process. Initially, Rogers RO4725JXR (Dk=2.55, Df 0.0026 at 10 GHz) was used with 15 µm Rogers 2626 (Dk=2.6, Df=0.003 at 10 GHz) as double-sided buildup layer for the simulations. The simulations were performed for both microstrip and CBCPW lines with and without the buildup layers.

3.5.2 Simulations with Laminate Stack-Up

The laminate stackup is shown in Figure 29. The figure depicts a cross-section rotated by 90 degrees to show signal path in red. This stackup is used for both microstrip and CBCPW simulations. It can be noted that the stackup height is the same as the glass TV that was fabricated, that is, 130 µm. No vias are used in the microstrip simulations. In case of simulations with bare laminates, no build-up layers are used.

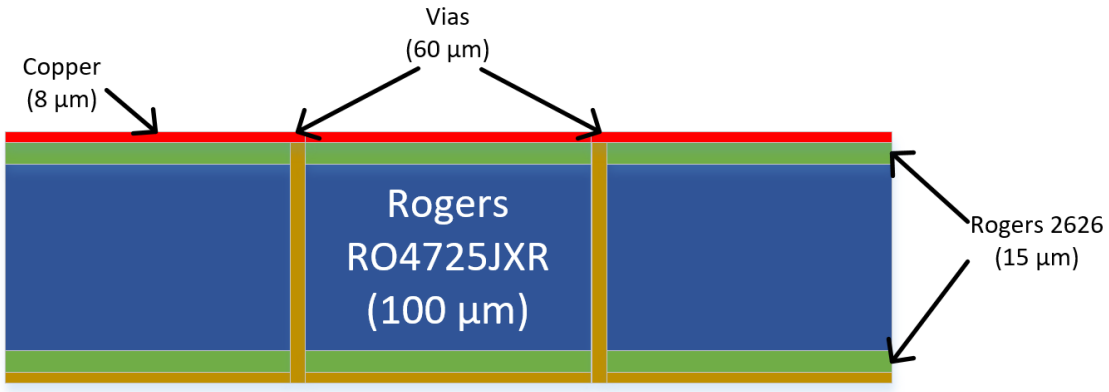


Figure 29: Laminate stackup for TL loss simulations.

The simulation was performed in Keysight's Advanced Design Systems (ADS) software with a frequency sweep from 40 MHz to 30 GHz. The number of cells per wavelength was set to 40 with an arc resolution of 10^0 in the preprocessor to accommodate for a finer mesh when using CBCPW lines. The first set of simulations was performed on bare laminate. The substrate definition is shown in Figure 30.

The core height was adjusted to 130 µm to keep consistency with the fabricated TV. For microstrip, the line width came out to be 355.8 µm for a 50 Ω line. The 3D EM preview of the simulated microstrip lines is shown in Figure 31 along with the results. The loss results of the simulation are numerically compiled in Table 11.

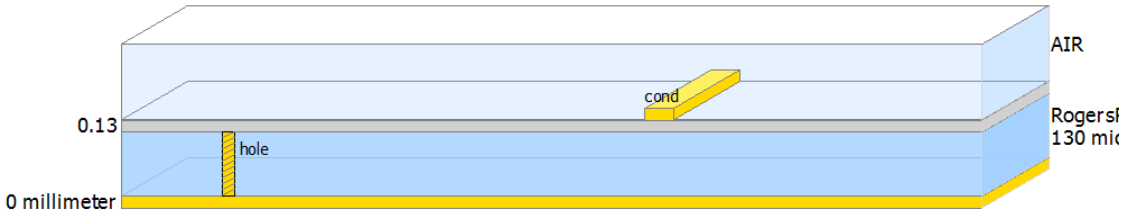
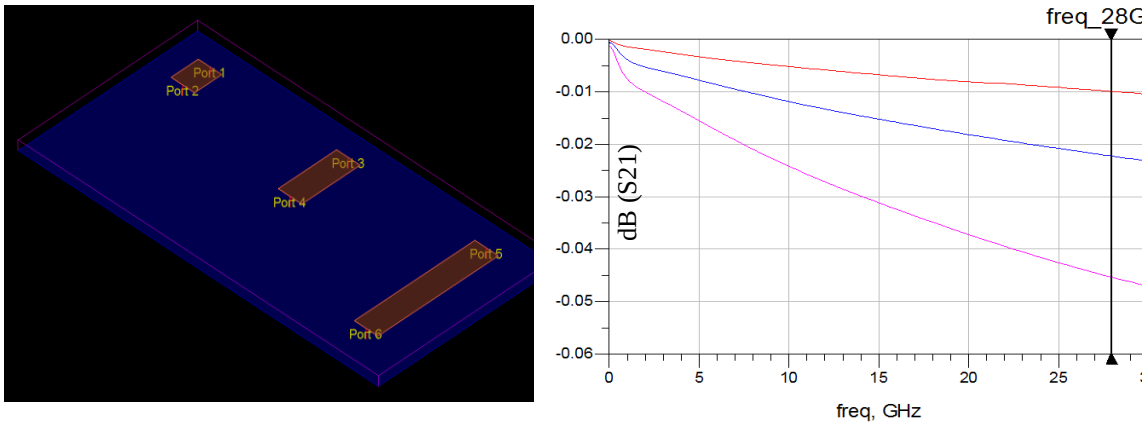


Figure 30: Substrate definition for simulation with bare laminates.



(a) (b)

Figure 31: (a) 3D EM preview of simulated microstrip lines on bare laminate (b) Simulation Results.

Table 11: Insertion loss for microstrip simulation on bare laminate.

Name	Loss (dB) at 28 GHz
Quarter	-0.010
Half	-0.022
Full	-0.045

Moving on to the simulation of microstrip on laminate stackup with buildup layer, the substrate definition changed as shown in Figure 32. Once again, the substrate thickness was kept at 130 µm to maintain consistency. This time the microstrip line width changed to 350 µm. The 3D EM preview and the results of this simulation are shown in Figure 33 along with the simulation results in Table 12.

Table 12: Insertion loss from simulations of microstrip on laminate with buildup.

Name	Loss (dB) at 28 GHz
Quarter	-0.015
Half	-0.030
Full	-0.049

The final simulation on laminate stackup was with CBCPW lines. The same substrate definition was used as shown in Figure 29. The width of the signal line was kept at 44 µm as in the case of glass TV. The signal-to-ground spacing was adjusted to 85.25 µm to maintain 50 Ω impedance. The via diameters were also kept consistent at 60 µm.

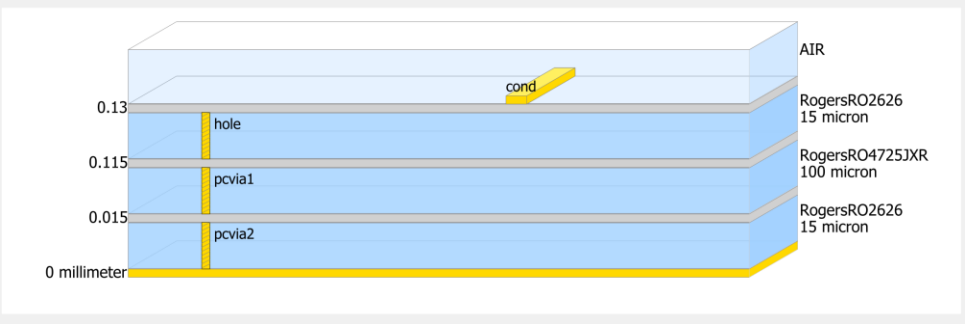
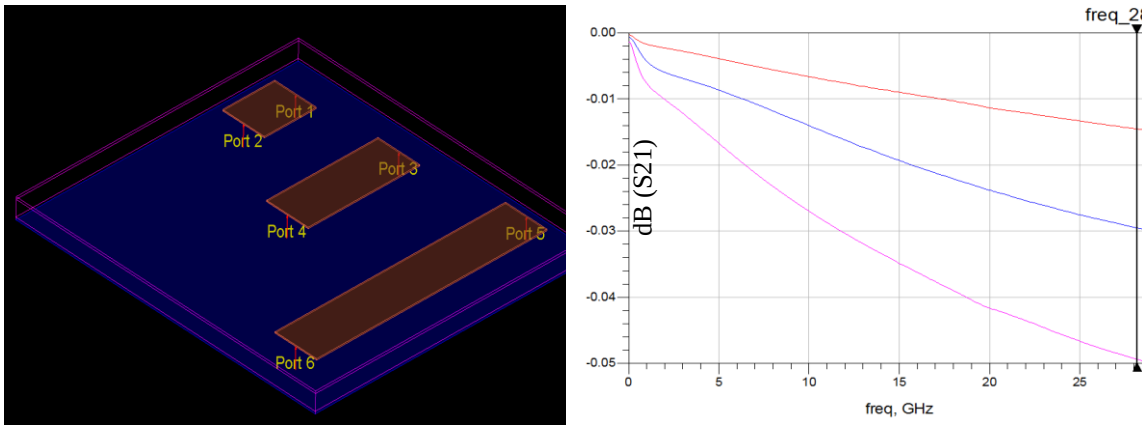


Figure 32: Substrate definition for simulations on laminate with buildup.



(a) (b)

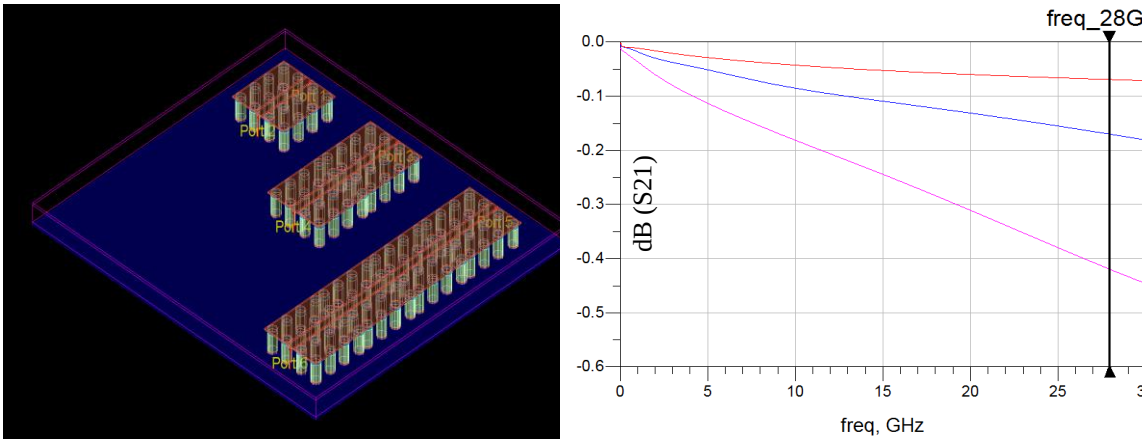
Figure 33: (a) 3D EM preview of simulated microstrip lines on laminate with buildup (b) Simulation results.

The 3D EM preview and results of this simulation are shown in Figure 34 along with the simulation results in Table 13.

It is interesting to note the increased loss in CBCPW with laminate stack-up. The difference of line widths: 350 µm for microstrip vs. 44 µm on CBCPW plays a very important role in the loss contributions.

Table 13: Insertion loss for CBCPW simulation on laminate with buildup.

Name	Loss (dB) at 28 GHz
Quarter	-0.069
Half	-0.170
Full	-0.419



(a) (b)

Figure 34: (a) 3D EM preview of simulated CBCPW lines on laminate with buildup (b) Simulation results.

3.5.3 Simulations with Revised Laminate Stack-Up

The initial candidate substrate that was used for simulation, Rogers RO4725JXR, had limited availability in 100 µm thickness range. Therefore, a similar but more readily available organic laminate from Rogers Corp., Rogers RO4830 laminate, with Dk of 3.2 at 77 GHz and Df of 0.0033 at 10 GHz, is used. The minimum available thickness for this substrate is 127 µm which is comparable to the 130 µm glass TV. Moreover, the simulation frequency was increased to 40 GHz to get insertion loss data at 39 GHz band as well. The stackup for this new simulation setup is shown in Figure 35. The length of lines chosen for

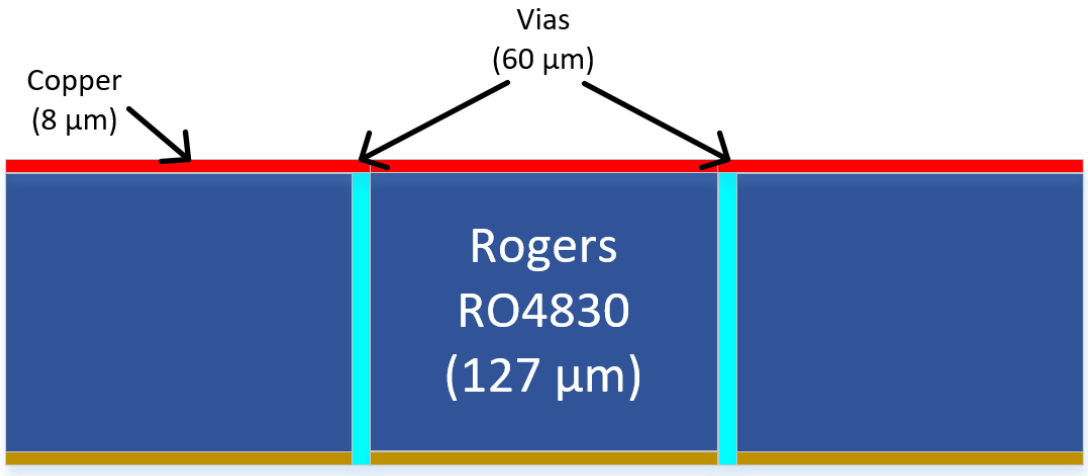
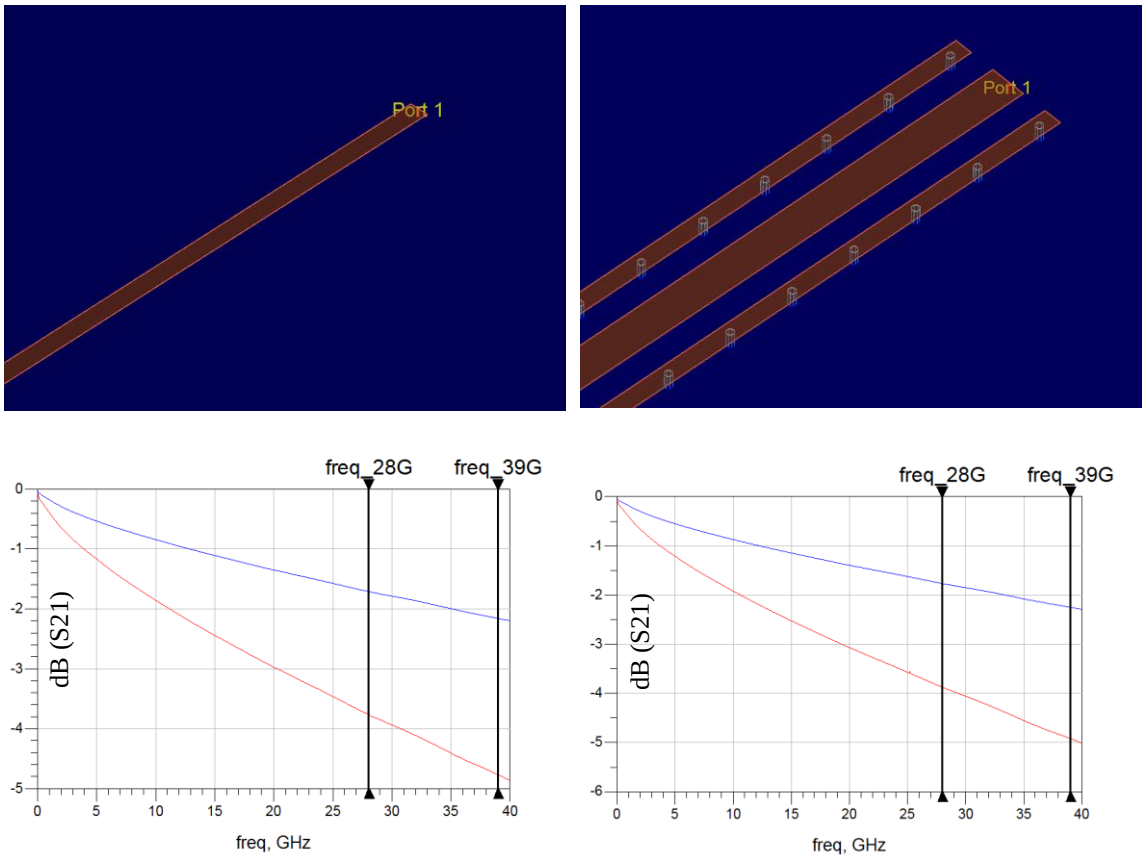


Figure 35: **New laminate stackup for TL loss simulations.**

this simulation was 11.0 mm and 5.0 mm, which correspond to full length and slightly less than half length of the mask. Length of 50 mm corresponds to 4.67λ at 28 GHz and 6.5λ at 39 GHz. Similarly, length of 110 mm corresponds to 10.27λ and 14.3λ at 39 GHz.

The results from these simulations are shown in Figure 36 and numerically compiled in Table 14. These results show that for a stackup with multilayered thick cores, laminates can be a good option for 5G applications.



(a) (b)

Figure 36: **3D EM view and insertion loss of new laminate stackup: (a) microstrip and (b) CBCPW.**

Table 14: Insertion loss from simulation with new laminate stackup.

Stackup	Length (mm)	Absolute Loss		Loss in dB/mm	
		28 GHz	39 GHz	28 GHz	39 GHz
Microstrip on Laminate (Simulated)	50	1.712	2.159	0.0342	0.0432
	110	3.765	4.770	0.0342	0.0434
CB-CPW on Laminate (Simulated)	50	1.769	2.253	0.0354	0.0451
	110	3.876	4.921	0.0352	0.0447

3.5.4 Simulations with Glass Stack-Up

Similar simulations were performed on glass while only changing the stack-up. The simulations were only performed on bare glass of 130 µm thickness, consistent with the fabricated TV. The glass stackup is shown in Figure 37.

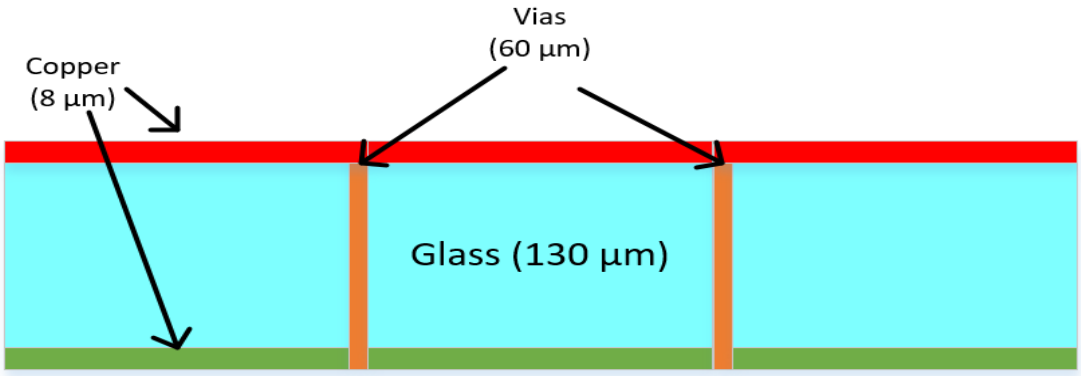
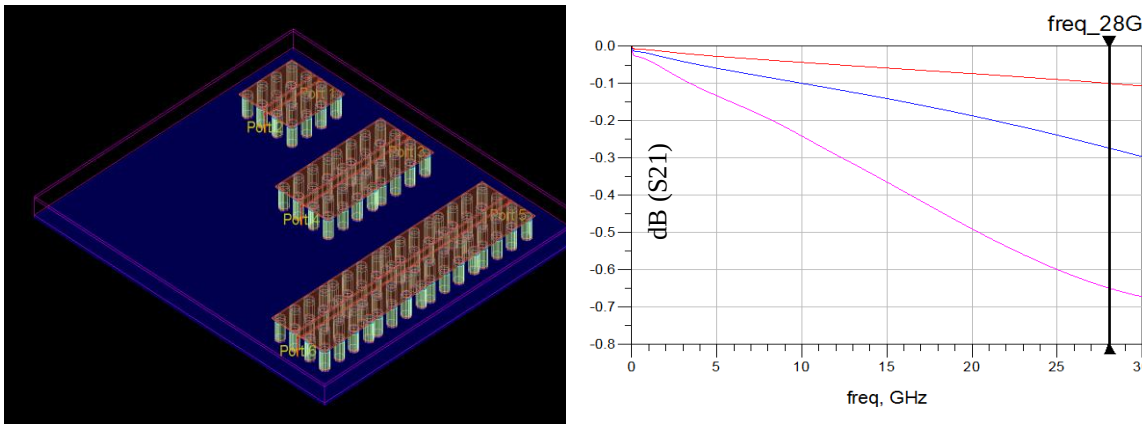


Figure 37: Glass stackup used in simulation.



(a) (b)

Figure 38: (a) 3D EM preview of simulated CB-CPW lines on glass stackup (b) Simulation results.

The signal path is shown in red. The simulation setup was the same as used for laminate stack-up simulations: same cells per wavelength and arc resolution criteria was maintained. The first set of simulations was for the CB-CPW lines on bare glass. In this case, the width of signal path was maintained at 44 µm but the signal-to-ground spacing was adjusted to 70 µm to maintain 50 Ω impedance. The 3D EM preview is shown in Figure 38 and the simulation results are numerically mentioned in Table 15.

Table 15: Insertion loss for CBCPW simulation on glass.

Name	Loss (dB) at 28 GHz
Quarter	-0.100
Half	-0.273
Full	-0.649

3.6 Glass substrate test-vehicle design

AGC glass of 130 μm thickness was used as the 5G substrate core. Since this fabrication presented an opportunity to test TL loss, several conductor-backed coplanar waveguides (CBCPW) were included in the 6” by 6” glass panel. The designed test-vehicle is shown in Figure 39.

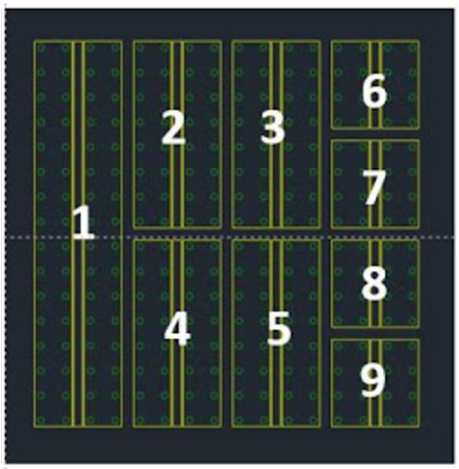


Figure 39: CBCPW Glass Test Vehicle.

3.7 Fabrication and Characterization of Transmission Line Test-Structures

3.7.1 Fabrication Process

Semi-Additive Patterning (SAP) process is used to fabricate 5G structures on glass panel. Appropriate handling procedures are required for glass substrate fabrication process to address the brittleness and fragility of ultrathin glass. Polymer lamination on glass is the key to address the challenges with glass handling and metallization of smooth glass surfaces. Low-modulus polymer also acts as a buffer layer that reduces the stress from high CTE copper on glass. Polymer films also enable metallization by acting as an adhesion-

promoting layer between electroless copper and glass. In addition, polymer acts as a barrier to prevent copper migration on glass surface between high density wiring under electrical bias. The glass panels are treated with silane to increase adhesion, and prevent delamination during subsequent wet processes. Ajinomoto's (ABF) GY-11 organic dry films with low dielectric loss of 0.0042 (5.8 GHz) are used in this test vehicle. Polymer lamination is performed with a vacuum laminator, followed by polymer curing. On the laminated polymer, a copper seed layer with a thickness of 0.2 μm is uniformly deposited. Adhesion of electroless copper to polymer is improved by prior roughening of the polymer surface using a permanganate chemical etch to create mechanical anchor sites. The wet chemical etch also cleans the residual polymer left on the nearby copper during via drilling processes. Metallization of top and bottom most metal traces and microvias is performed using a semi-additive patterning (SAP) process. Unlike a subtractive patterning, where a thick copper foil is etched off from the undesired areas to form circuit patterns, SAP yields better dimensional and copper sidewall control. This is because SAP avoids the long etching and lateral undercut that is usually prevalent during subtractive etching. This process flow is applied to fabricate patch antenna test-structures described in Chapter 4 [35]. The CBCPW structures are fabricated by a simpler process comprising of direct Ti/Cu sputtering on bare glass and SAP. This process flow is shown in Figure 40.

3.7.2 Characterization of Glass Substrates

Three similar glass TVs were fabricated and a total of 13 coupons were measured. The results of glass TV coupon in Figure 39 are shown in Figure 42 with loss values in Table 16. Figure 42 shows three cases of quarter-, two cases of half- and one case of full-length

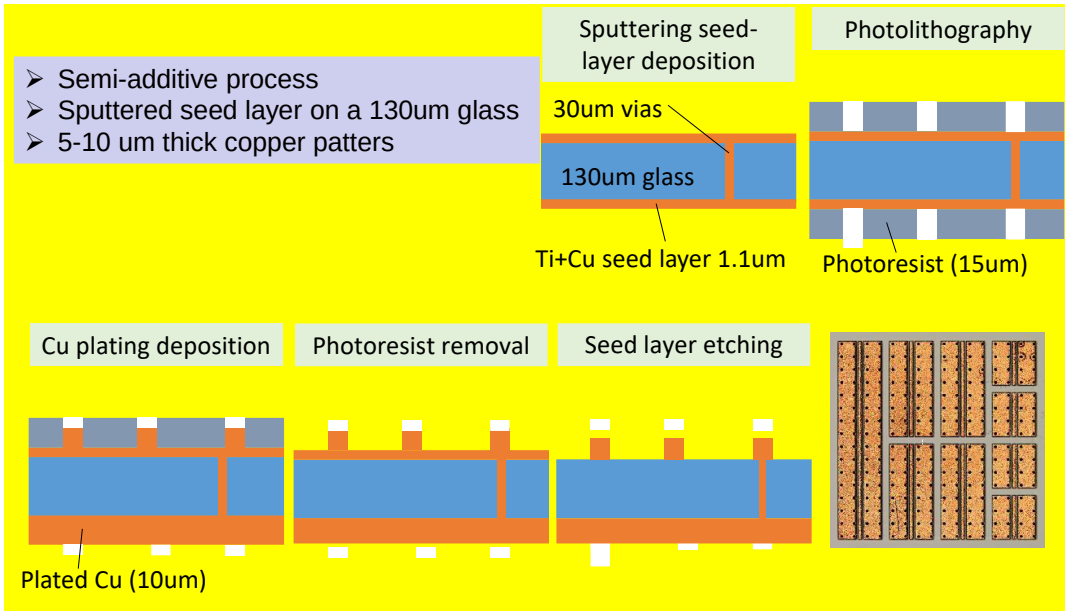


Figure 40: A typical process flow for fabrication of organic substrates.

CBCPWs and these include the worst-case loss observed during the measurements. The sample data was tabulated to compute mean and standard deviation to give a better idea of the overall measured data. The setup used to measure the samples is in Athena Lab of Georgia Tech. The setup includes a probe station connected to VNA from Anritsu (Model no. 37269B) with a frequency range of 40 MHz to 40 GHz. For measurement, 500 µm pitch Ground-Signal-Ground probes by Cascade Microtech along with their calibration kit are utilized. A SOLT calibration procedure is (Short-Open-Load-Through) used for the whole frequency range of VNA. SMA-styled 2.92 mm connector cables are used to connect VNA ports to probing station ports. The setup is shown in Figure 41 and the measured data is summarized in Table 17.

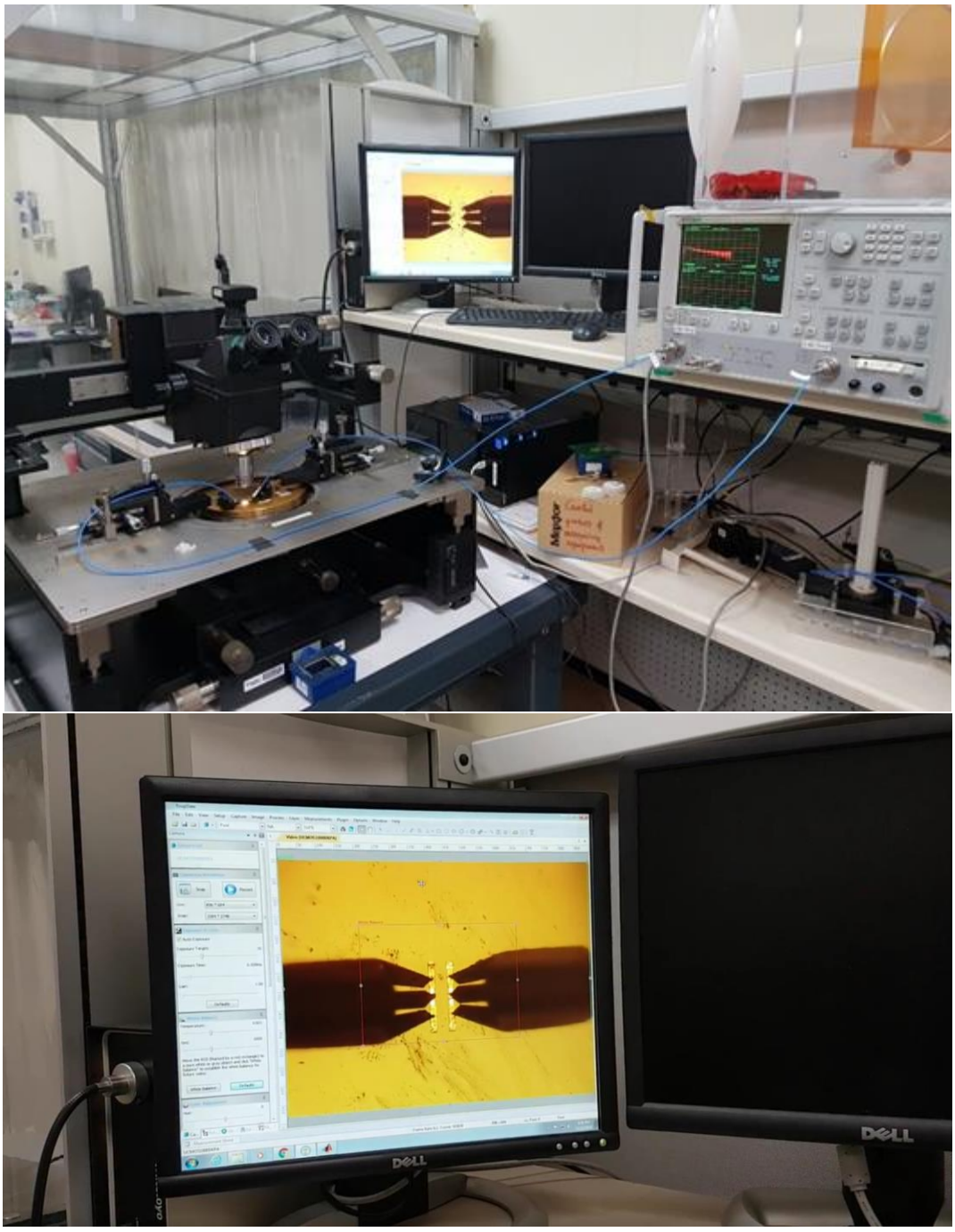


Figure 41: Probing station and VNA setup in Athena lab at Georgia Tech.

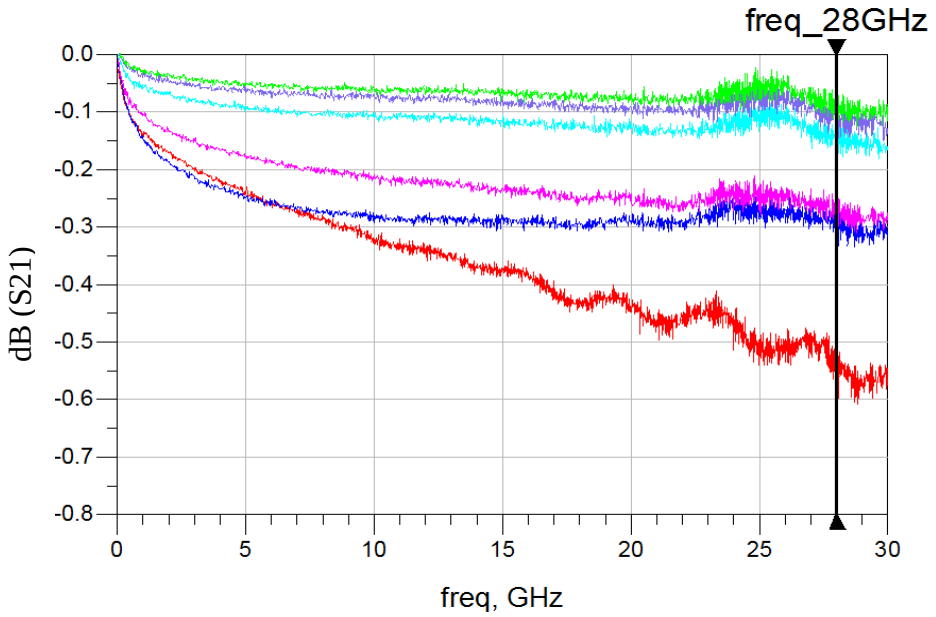


Figure 42: Measured results from CBCPW glass TV coupons.

Table 16: Measured insertion loss for CBCPW from fabricated glass TVs.

Name	Loss (dB) at 28 GHz
Quarter	-0.089
	-0.101
	-0.140
Half	-0.264
	-0.298
Full	-0.532

A more meaningful insight of the simulation data can be observed when the loss is calculated as dB/mm. This data was compiled for all the simulations and only the worst case is considered in case of the measured results, and are shown in Figure 43. A comparison of all simulation results is shown in Table 18.

Table 17: Mean and standard deviation of loss in dB/mm for glass TVs.

Line Lengths	Mean Loss (dB)	Mean Loss in dB/mm	Standard Deviation
Quarter	-0.078	0.186	7.32%
Half	-0.186	0.208	6.59%
Full	-0.447	0.240	3.06%

The fabricated sample along with a zoomed in view is shown in Figure 43.

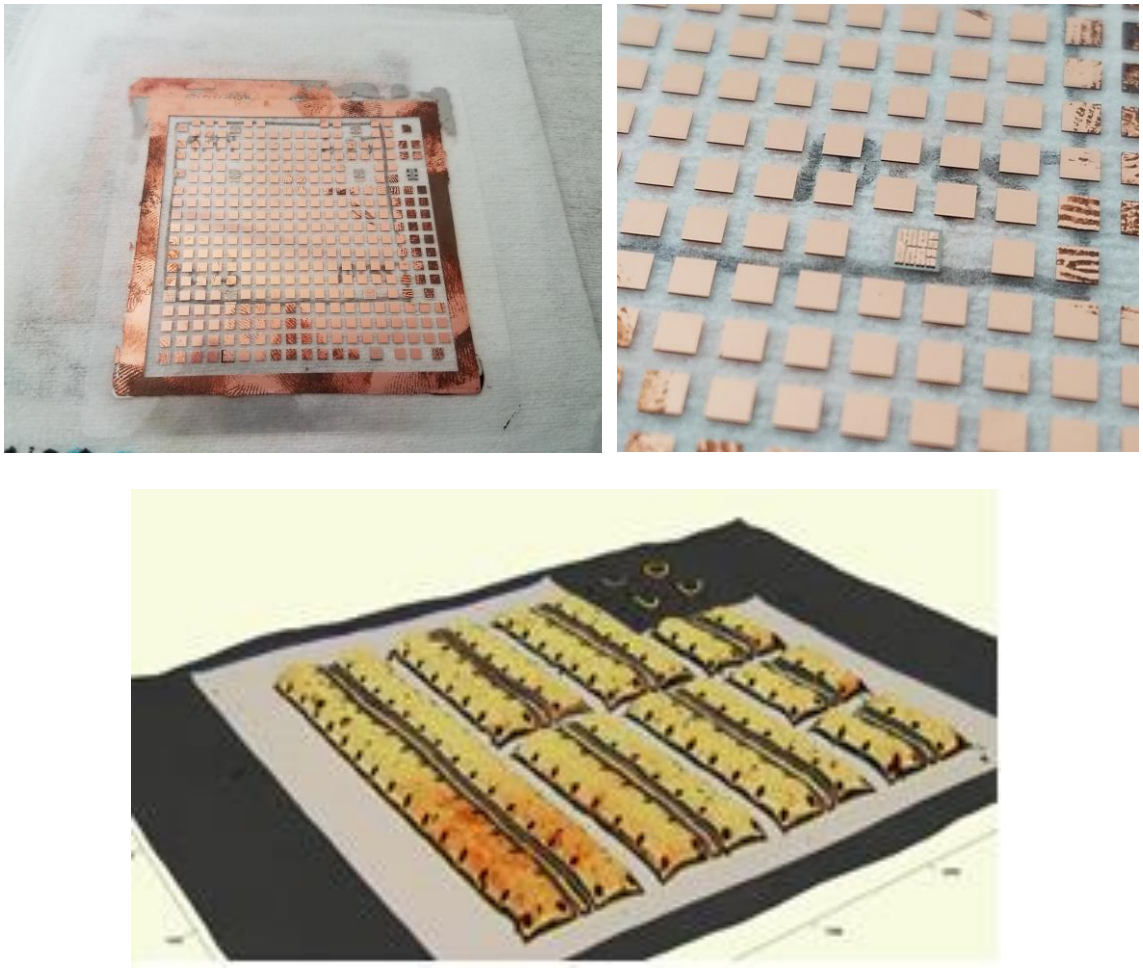


Figure 43: Fabricated glass TV and coupons.

Table 18: Simulated and measured results for loss in dB/mm.

Stackup	Length	Absolute Loss at 28 GHz	Loss in dB/mm
Microstrip Laminate without buildup (Simulated)	Quarter	0.010	0.024
	Half	0.020	0.022
	Full	0.045	0.024
Microstrip Laminate with buildup (Simulated)	Quarter	0.015	0.036
	Half	0.030	0.033
	Full	0.049	0.026
CB-CPW Laminate (Simulated)	Quarter	0.070	0.167
	Half	0.140	0.167
	Full	0.289	0.172
CB-CPW Glass (Simulated)	Quarter	0.100	0.238
	Half	0.273	0.303
	Full	0.649	0.349
CB-CPW Glass (Measured)	Quarter	0.140	0.333
	Half	0.298	0.331
	Full	0.532	0.286

3.7.3 Analysis of Simulated and Measured Results

As evident from data in Table 18, the loss target is only achieved in microstrip simulations on laminate with and without buildup. This kind of response was expected due to the very low loss tangent of Rogers RO4725JXR. The simulation and measurement results on glass match to a certain extent. The wavelength at 28 GHz is 10.71 mm and the longest fabricated

line, termed as full-length, is 1.86 mm long, which is less than a quarter wavelength. A smaller length can overshadow the actual loss in dB/mm on a substrate. A longer line length that is multiples of the wavelength of frequency of interest would give a more reasonable data. Simulations with longer line lengths would performed as the next step.

3.8 Summary

Various substrate technologies: organic laminates, LTCC and glass were benchmarked against each other in terms of their electrical properties and processability. The key benefits and current shortcomings of each candidates are discussed. A library of qualifying materials for both core and RDL was compiled. From these candidate materials, upto 18 combinations of core and RDL were considered, from which, three combinations were down-selected. Glass test-vehicles with CBCPW transmission lines of various lengths were modeled, designed and fabricated. Same line lengths were used on other combinations of substrates. The measured results are tabulated as mean and worst-case losses in dB/mm for all the three CBCPW lengths. The responses are spread across a standard deviation of 7.32% in case of shortest length of TL, which indicates a high level of consistency in the measurement data.

CHAPTER 4

MODEL-TO-HARWARE CORRELATION STUDY

The objective of this task is to investigate the validity of 5G models and quantify the effect of process variation on performance deviation. Microstrip-fed rectangular patch antennas are chosen for model-to-hardware correlation study as they form the most fundamental antenna elements. Studies with patch antennas can then be extended to advanced feedlines for wide-band phase-shifting networks. The sensitivity of measurements to geometry, probing and material properties is also shown through far-end cross-talk measurements from 1-5 GHz between two transmission lines.

For the best system performance, antennas need to be integrated onto the substrate with active circuits using low-loss interconnections and feedlines. Glass enables transmission lines with high precision, tolerance and low loss for miniaturized antenna array module with double-side thin-film components. Therefore, glass is used as the substrate for this task. Single-element patch antennas are used as the test-structure. Grouping these antenna elements together will results in several advantageous properties such as higher directivity compared to a single antenna element, which is not the focus of this work.

4.1 Modeling and Characterization of Microstrip Rectangular Patch Antenna Test Vehicle

Out of the several variations of microstrip patch antennas, edge-fed rectangular patch antenna was chosen because of its simplicity in design. The antenna with nomenclature of its dimensions is shown in Figure 44.

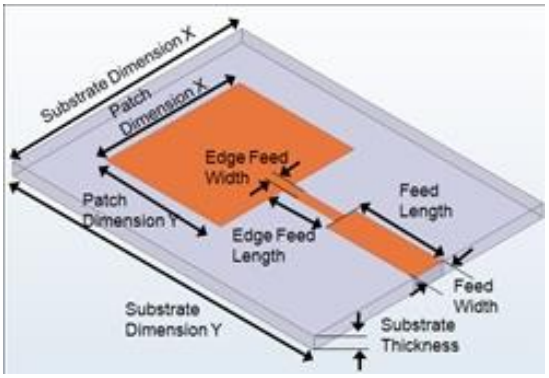


Figure 44: Rectangular edge-fed patch-antenna.

A frequency range of 37.5-39 GHz was chosen for the designs. The rectangular patch antenna is approximately a one-half wavelength long section of a rectangular microstrip transmission line. When air is assumed as its substrate, the length of the rectangular microstrip antenna is approximately one-half of the free-space wavelength corresponding to its operating frequency. The length of the antenna decreases as 1/sqrt(Dk) when it is loaded with a dielectric substrate of dielectric constant (Dk). The resonant length of the antenna is slightly shorter because of the extended electric fringing fields which slightly increase the electrical length of the antenna.

Several theories can be used to analyze and design a rectangular microstrip patch antenna. These include transmission line mode, cavity model etc. Transmission line model design technique will be used in this work. According to this technique, a rectangular patch of length L and width W can be viewed as a very wide transmission line that is transversely resonating. The electric field varies in a sinusoidal fashion under the patch along its resonant length L. It is assumed that the electric field does not change along the width of the patch antenna. Moreover, it is assumed that the radiation comes from the fields leaking out the width or radiating edges of the antenna. For an effective radiator, a practical width

that leads to good radiation efficiencies for fundamental TM_{10} mode is given by Equation 2.

$$W = \frac{c}{2f\left[\frac{\varepsilon_r + 1}{2}\right]^{1/2}} \tag{2}$$

The effective dielectric constant ε_{eff} for a microstrip is given in Equation 3.

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + \frac{12h}{w}\right)^{-\frac{1}{2}}\right] for\ w/h \geq 1 \tag{3}$$

Since microstrip has fringing fields and quasi-TEM modes, the electrical length of the patch appears slightly larger than its physical length, which requires a correction term ΔL, also known as Edge Extension, to account for the fringe capacitance. This edge extension is defined in Equation 4.

$$\Delta L = 0.412h\left[\left(\frac{\varepsilon_{eff} + 0.3}{\varepsilon_{eff} - 0.258}\right)\left(\frac{\frac{w}{h} + 0.264}{\frac{w}{h} + 0.813}\right)\right] \tag{4}$$

where h is the substrate height and w is the width of the transmission line. Because of the fringing effect, the length of the patch is extended on each side by ΔL. Therefore, the effective length is given by Equation 5.

$$L_{eff} = L + 2\Delta L \tag{5}$$

In order to resonate, this length must be equal to half wavelength corresponding to the design frequency. Mathematically:

$$f_r = \frac{c}{2L_{eff}\sqrt{\varepsilon_{eff}}} \tag{6}$$

For a TM_{mn} mode, the resonant frequency can be calculated for a given length L by the following equation:

$$f_r = \frac{c}{2\sqrt{\varepsilon_{eff}}}\left[\left(\frac{m}{L}\right)^2 + \left(\frac{n}{W}\right)^2\right]^{1/2} \tag{7}$$

After finding the actual length of the patch, the desired rectangular microstrip patch antenna is designed. The antenna edge impedance is calculated using an online calculator and then a quarter-wave transformer is designed to match it to the characteristic impedance of 50 Ω. AGC ultra-thin glass with 100 μm thickness is used as the substrate. It has Dk of 5.41 and Df of 0.009 at 35 GHz. A thin layer of polymer, ABF GY-11 thin-film with 15 μm thickness, is laminated onto both sides of the glass for better handling and processing. It has Dk of 3.2 and Df of 0.0042 at 10 GHz. The stackup used for antenna simulation is shown in Figure 45. The final antenna dimensions are given in Table 19. These dimensions are obtained after optimization and correlation from online calculators and HFSS Antenna Design Kit (ADK). HFSS from ANSYS is used as the modeling software for this test structure.

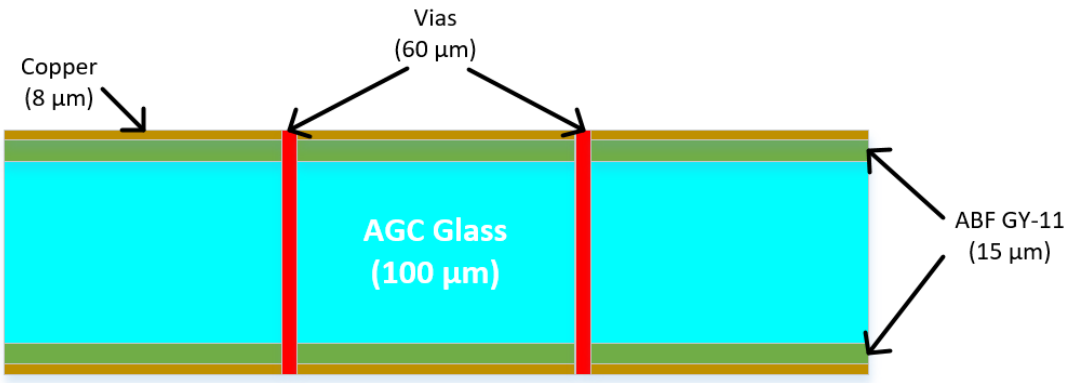


Figure 45: Glass stackup used for antenna modeling and fabrication.

Table 19: Dimensions of patch antennas at four different resonant frequencies.

Antenna	Center Frequency	Patch Dimension		Feedline Dimension	
	(GHz)	Width (µm)	Length (µm)	Width (µm)	Length (µm)
Patch A	37.5	2170	1800	29	1033
Patch B	38.0		1770		
Patch C	38.5		1750		
Patch D	39.0		1720		

As inferred from the table, only the length of the patch is changed to adjust the resonant frequency, which makes the antenna sensitive to this dimension. This implies that the probability of discrepancy between model and hardware, if any, increases due to the variation in this specific dimension of the antenna. The simulation results of all antennas are shown in Figure 46.

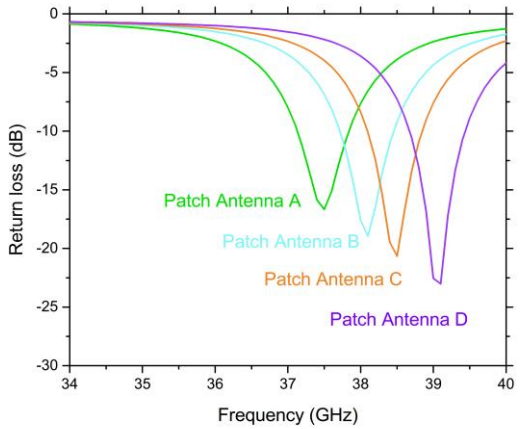


Figure 46: Simulation results of rectangular patch antennas.

The antennas show a 3-dB bandwidth of 6.4-6.7%. The antenna panels are fabricated using the SAP method explained in chapter 2. The fabricated panel is shown in Figure 47.

The ground pads are added as a utility to ensure that the antennas are measurable on the probe-station VNA setup at Athena Lab in Georgia Tech. These pads are also a part of simulation and they were placed at 220 μm from the edge of 50 Ω line. The choice of this distance ensures that the characteristic impedance line stays at its impedance and a 250-500 μm GSG probe can be used to test this panel. All the panels are tested with a single calibration to remove any uncertainty in the measurement data. The measured data of each antenna is shown in Figure 48 and the numerical data is given in Table 20. Three out of all the measured samples of each antenna are plotted along with the simulation results. The key observations from the measurements are:

- The antennas shifted to lower frequencies
- The measured antennas are mostly consistent with their resonant frequency

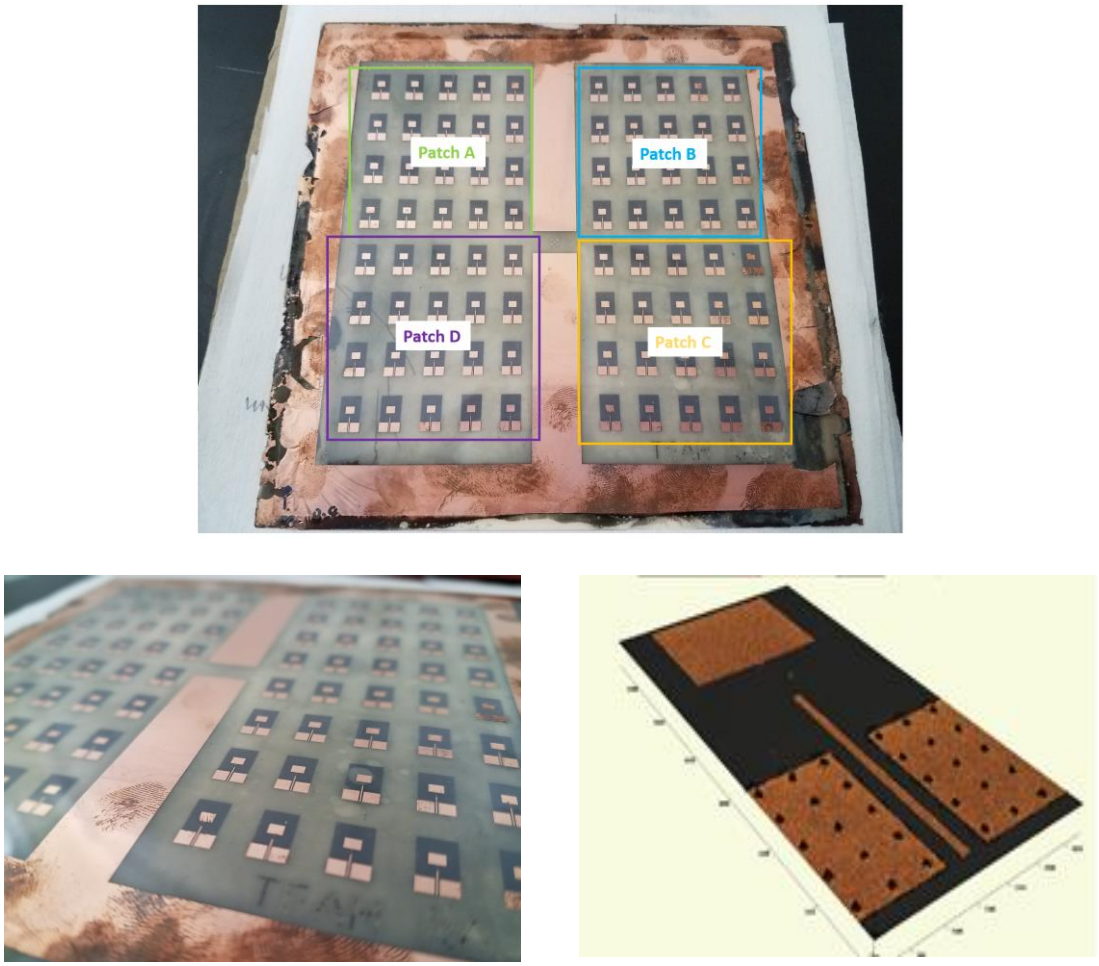


Figure 47: Fabricated patch antennas on glass panel.

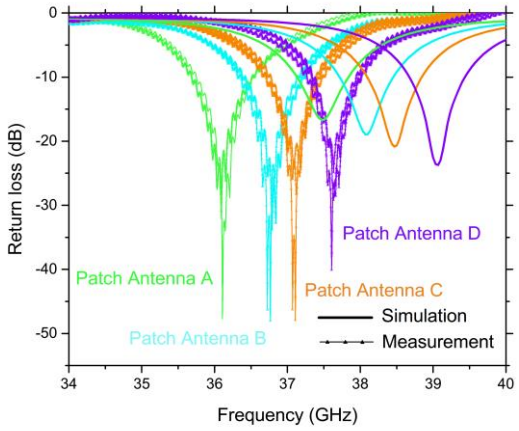


Figure 48: Measured results from patch antennas.

Table 20: Numerical measured data of patch antenna testing.

Antenna Frequency (GHz)	Number of Samples Measured	Mean Resonance Frequency (GHz)	Mean Return Loss (dB)	Standard Deviation in Resonance Frequency	Mean Difference from Design Frequency (GHz)
37.5	20	35.892	-32.56	11.94%	-1.608
38	20	36.61	-35.244	17.31%	-1.386
38.5	19	36.73	-35.244	35.93%	-1.773
39	19	37.41	-27.922	14.86%	-1.594

The standard deviation data shows that only 38.5 GHz antenna has a large spread of resonant frequencies, while the rest of the antennas have their resonant frequencies in a narrow range. In order to identify the origin of frequency shift, each dimension is measured and tabulated against the designed dimensions in Table 21.

Model-to-hardware correlation

The measured shift in performance is unacceptable for 5G, and, therefore, brings out a variety of factors that need to be addressed. The first factor is that the antenna resonant frequency is extremely sensitive to its length. A variation of 20-30 μm is enough to shift the resonant frequency of the antenna by 500 MHz, as depicted numerically in the design parameters table. The coupons that match each other are dimensionally consistent and most of them showed a frequency shift 1.4 GHz. Secondly, the simulations verified that the width of the quarter-wave transformer is not a major contributor to the frequency shift.

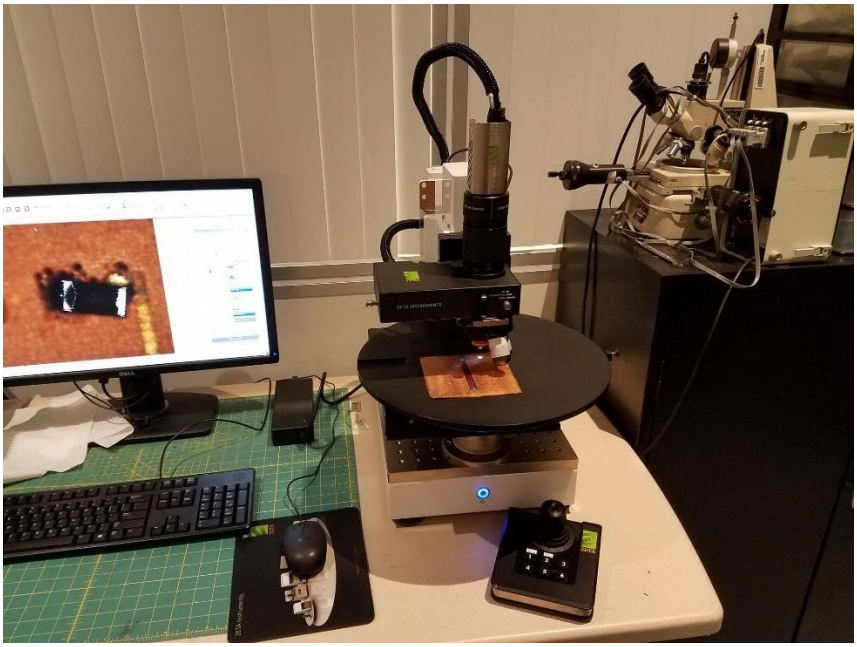


Figure 49: Laser confocal scanning to measure the geometries of the test-structures.

The measurement setup for dimensional analysis is shown in Figure 49. The method of image stitching was used to measure the antenna dimensions using a 50X zoom lens. The method itself can bring an error of 5-10 μm in the measurements [35].

A set of simulations was performed to see if the dimensional variations alone can justify the simulation. Unfortunately, they do not give as large a shift as observed in the measured results. This begs the question about the veracity of electrical properties and thickness used for simulations. The same set of simulations was performed with a range of Dk values to identify if the error in Dk is the reason for such a large shift. Simulations with a Dk value of 6.2 at 35 GHz exactly match with the measurements for all the antennas, with the assumption that the shift in each antenna is 1.4 GHz. However, error in Dk cannot be the only contributor to the shift as there are uncertainties associated with the thickness variations of the substrate as well as the deposited copper. Identifying and quantifying the

Table 21: Dimensional comparison between designed and fabricated patch antennas.

Parameter	Patch A (37.5 GHz)		Patch B (38.0 GHz)	
(μm)	Simulated	Measured	Simulated	Measured
Patch Width	2170	2164	2170	2163
Patch Length	1800	1791	1770	1763
Feedline Width	29	23.7	29	24.5
Feedline Length	1033	1039	1033	1045
	Patch C (38.5 GHz)		Patch D (39.0 GHz)	
Patch Width	2170	2164	2170	2162
Patch Length	1750	1742	1720	1711
Feedline Width	29	23.7	29	23.9
Feedline Length	1033	1044	1033	1041

origin of the shift is imperative and it requires an extensive study involving both modeling and fabrication.

The re-simulated antenna results are shown along with the measured results in Figure 50. The factors associated with the frequency shift in the measured results are summarized as:

- Uncertainty in the electrical properties of the substrates at higher frequencies
- Dimensional variation caused by the fabrication process
- Variation in substrate thickness as well as deposited copper thickness

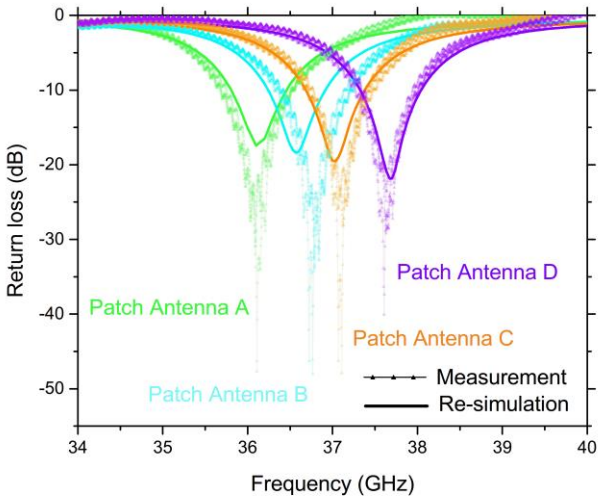


Figure 50: Re-simulated frequency response of patch antennas.

4.2 Model-to-Hardware Correlation with Coupled Microstrip Lines

Redistribution layers (RDL) have metal traces in a dielectric medium that either re-route the interconnections to a uniform and coarse pitch on the IC side, or provide intra-chip and inter-chip communication in the package side. In RF substrates, RDL supports the transmission lines, I/O routing from the transceiver chip to the antenna along with variety of passive components. With the advancements in package substrate technologies, RDL is becoming increasingly important to not only route fine-pitch I/Os but also facilitate the strict design rules required for precision impedance. RDL height in typical RF substrates generally ranges from 15 to 80 μm. RDL dielectrics need to have excellent adhesion to core and is usually deposited by the process of lamination. The individual sheets can also be stacked to yield thicker adhesive layers.

The objective of this task is to model, design, fabricate and measure the far-end cross-talk between coupled lines from 1-5 GHz. The coupled lines are separated by a grounded-wall

to enhance the isolation between the two lines and reduce the coupling. This model-to-hardware correlation study is performed at lower IF bands as compared to 5G. IF bands are employed in a heterogeneous receiver, where a Local Oscillator (LO) is mixed with an input RF frequency. More specifically, the process of down-converting frequency from RF or carrier frequency to IF occurs in the superheterodyne mixer. The advantages of using IF bands for signal processing are easier handling, larger component size because of lower frequencies, and lower component cost. The coupled microstrip lines can be considered as a pair of power lines carrying high power IF signal. These lines need to be isolated from each other (less far-end cross-talk) to ensure high signal integrity and minimize coupling. Two cases are modeled:

Case-1: Matched coupled microstrip lines separated by 500 μm (edge-to-edge) and shielded with a grounded wall

Case-2: Matched coupled microstrip lines separated by 1500 μm (edge-to-edge) and shielded with a grounded wall

Rogers 2626 of 75 μm thickness is used as the RDL. It has Dk of 2.6 and Df of 0.003 at 10 GHz. It is used as a double-sided RDL with a Rogers core. The stackup is shown in Figure 51.

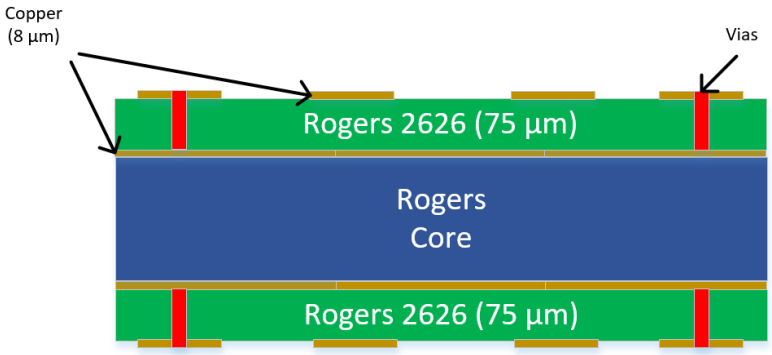
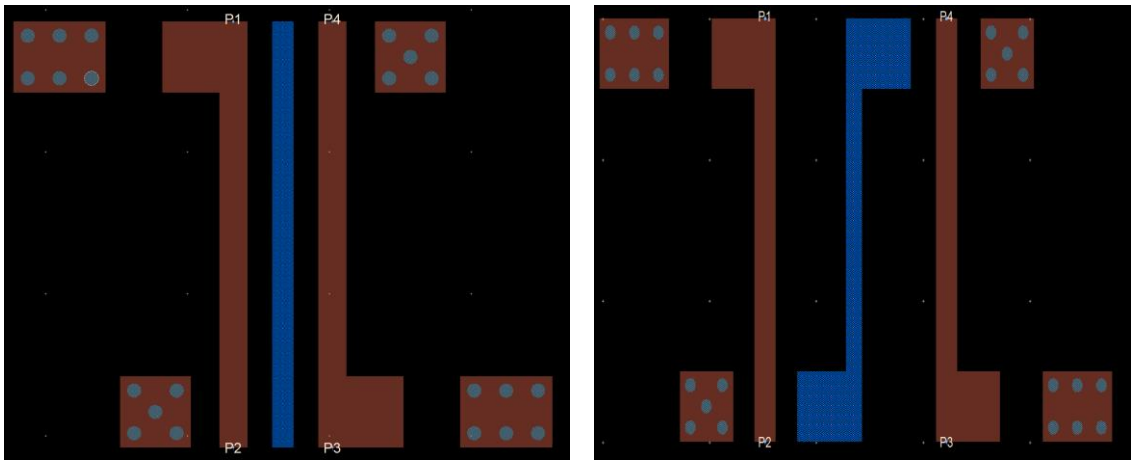


Figure 51: Stackup for RDL test vehicle.

ADS from Keysight Technologies was used as a simulation software. The layout for both structures is shown in Figure 52. The simulation setup is as follows:

- Frequency sweep: 1-5 GHz
- Cells per wavelength: 60
- Line width: 199 µm
- Conductor thickness: 8 µm

The simulation results are shown in Figure 53. The same SAP process, reported in the previous chapter, was used for fabrication of the these test vehicles. After the completion of the fabrication process, the next step is to solder termination resistors onto the microstrip coupled-lines and measure the far-end cross-talk. Surface Mount Device (SMD) resistors of 1005 metric size (1 mm by 0.5 mm) and 50 Ω impedance were used. Since the resistors are smaller in size, a conventional solder iron cannot be used. The process of reflow soldering is used to assemble the SMD components on a substrate. The goal of the process is to melt the solder paste and heat the adjoining surfaces without overheating and damaging the electrical components. The process is explained in detail below:



(a) (b)

Figure 52: Microstrip coupled-line on RDL test structures (a) Case-1: 500 µm spacing (b) Case-2: 1500 µm spacing.

- Solder paste, a sticky mixture of conductive paste and solder flux, is used to assemble the SMD components onto the substrate
- The substrate is placed in a reflow oven, which executes a reflow temperature profile shown in Figure 54

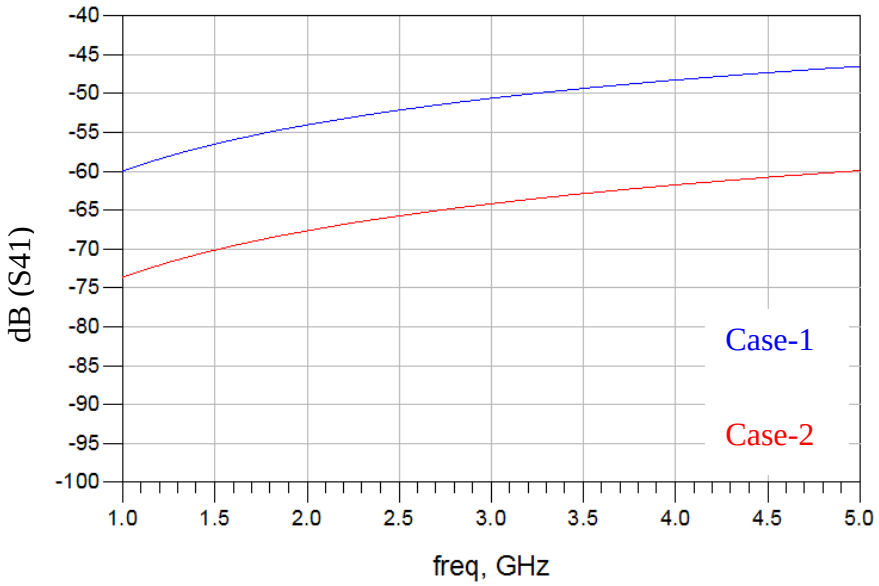


Figure 53: Simulation results of microstrip coupled-lines on RDL.

- There are four distinct temperature zones in a typical reflow solder profile:
    - Preheat Zone: It is the first stage of this process. The main goal of this process is to slowly raise the temperature of the whole sample to soak at pre-reflow temperature. It typically lasts for 75 seconds and the temperature slope is 1.0-2.0^{0}C/s
    - Thermal Soak Zone: The purpose of this zone is to activate the flux inside the solder paste. Typically, it lasts for 60-120 seconds and the temperature is maintained at 160 ± 5^{0}C
    - Reflow Zone: It is the third zone of the reflow process. The maximum allowable temperature is set in this zone and is usually kept much below the minimum critical operating temperature of a device in the whole system. This is where soldering happens and it lasts for 60-70 seconds
    - Cooling Zone: It is the final stage of the process and the sample is cooled down to room temperature at a rate of 4^{0}C/s

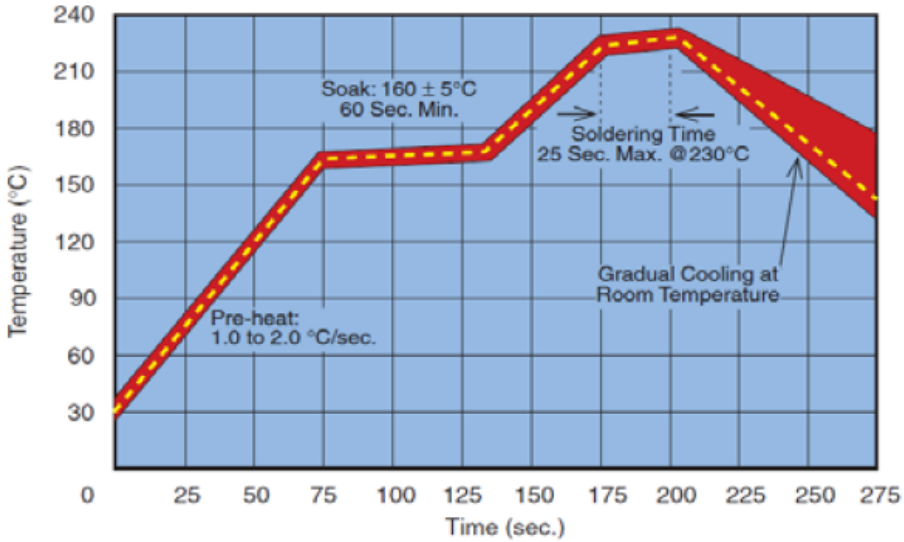


Figure 54: A typical reflow soldering temperature profile.

The fabricated samples after the terminations are shown in Figure 56.

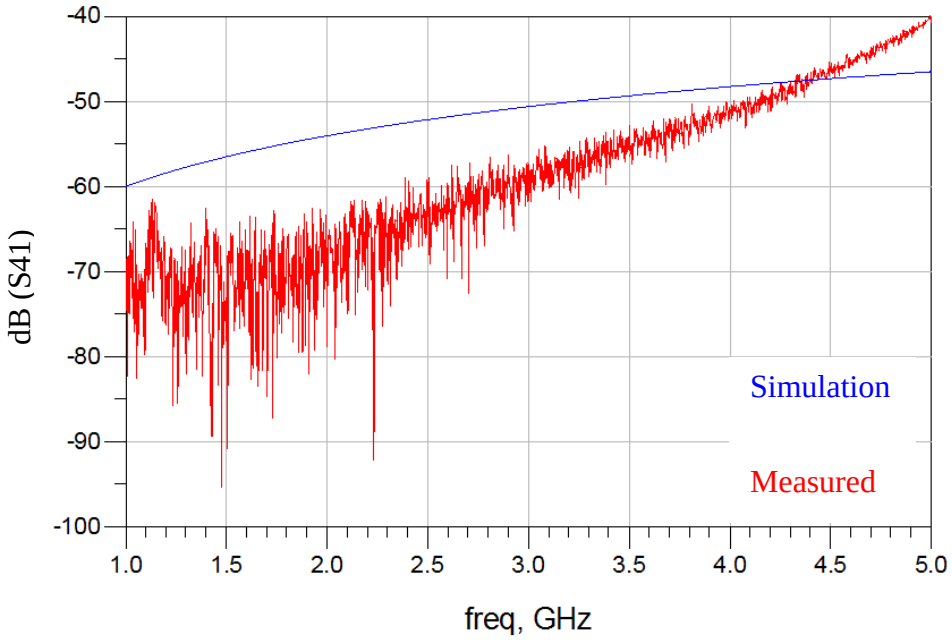


Figure 55: Simulation and measured results of coupled microstrip lines for Case-1.

Figure 56: RDL test vehicle after fabrication and reflow process.

Measurement Results

The measurement setup for characterization of RDL test vehicle is the same as that used for testing the transmission line and rectangular patch antenna test vehicles. The test results are shown are in Figure 55 and Figure 57.

Model-to-hardware correlations:

The difference in the simulated isolation performance between two cases is almost 15 dB over the whole frequency sweep. Case-1: 500 μm show a better correlation than Case-2: 1500 μm spacing. At lower frequencies of upto 3 GHz, the measurements match with simulations. At higher frequencies, the isolation between the coupled-lines decreases significantly in Case-2. Several reasons can lead to the decrease in isolation at higher frequencies for Case-2, such as improper grounding of the test coupons or the wall that separates the microstrip coupled lines. The noise floor of test equipment can be a limiting factor as well. However, excellent correlation between the simulation and measurements for Case-1 spacing shows that the excellent far-end cross-talk is more than -50 dB throughout the S-band. Similarly, a far-end cross-talk of more than -45 dB over the entire S-band is achieved in Case-2.

4.3 Summary

Model-to-hardware correlation study was performed on two structures: rectangular patch antennas and coupled microstrip lines. The structures were modeled, fabricated and characterized using EM simulators: HFSS and ADS, respectively. The results were compared with the simulation and the discrepancy is explained in terms of changes in electrical properties of glass at higher frequencies and small dimensional variations during the process. Therefore, testing at mm-wave frequencies requires a well-characterized test

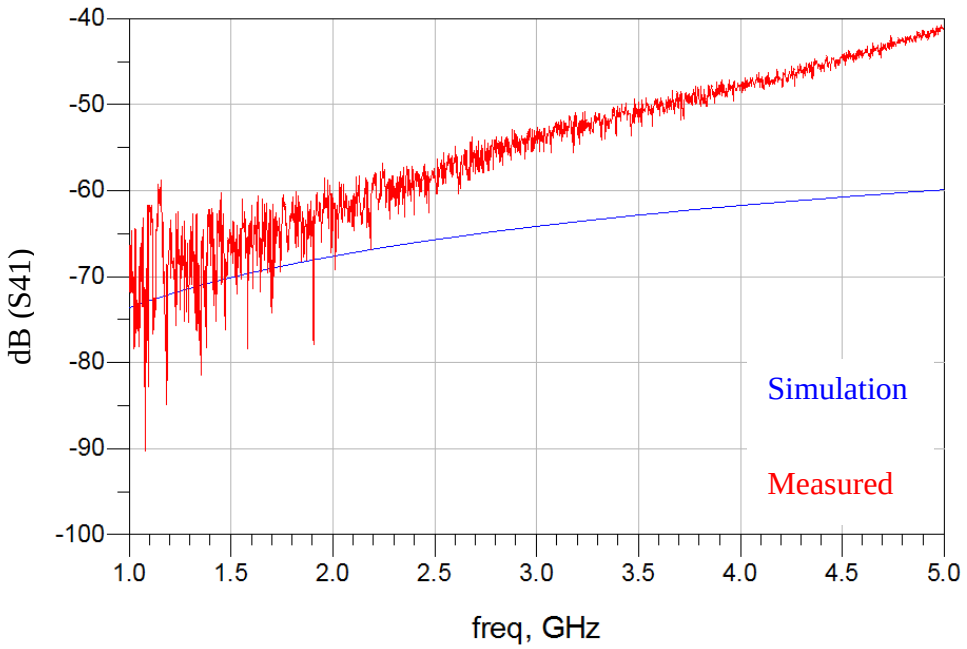


Figure 57: Simulation and measured results of coupled microstrip lines for Case-2.

bench with precise geometries and accurate properties. For the model-to-hardware correlation study using coupled microstrip lines, a good correlation was achieved between the model and hardware as revealed in the comparison of simulation and measured results.

CHAPTER 5

SUMMARY AND SUGGESTIONS FOR FUTURE WORK

The objectives of this research are to model, design, and develop advanced substrate technologies for 5G application in the Ka-band (26.5-40 GHz). The specific objectives are:

- Evaluate and identify different substrate candidates for 5G applications
- Design, fabricate and demonstrate low-loss transmission lines with 0.05 dB/mm with the front-up candidates
- Perform model-to-hardware correlation studies for 5G applications with advanced substrates

5.1 Advanced 5G Substrates and Low-Loss Transmission Lines

The objective is to evaluate and identify ideal material candidates for core and build-up layer materials to realize mm-wave package substrates. An extensive paper study was performed to evaluate several candidates for 5G substrates. The substrate technologies: organic laminates, LTCC and glass are benchmarked against each other. The key benefits and current shortcomings of each candidates are discussed. Structure or anatomy of package substrate for each technology is presented and analyzed. The process of making the package substrates is described with illustrations and figures.

A library of qualifying materials for both core and RDL was compiled. Out of those materials, upto 18 combinations of core and RDL were considered, from which, three combinations were down-selected.

Glass presents itself as an attractive emerging alternate to conventional substrate technologies as it has relatively low loss and a large panel size for lower cost can be achieved on it. It provides additional benefits such as superior dimensional stability, ability to form fine-pitch through-vias, stability to temperature and humidity variations and matched CTE with devices. Moreover, it has compatibility with advanced low-loss dielectric buildup materials. It enables precision circuitry and impedance control due to its high dimensional stability. It offers excellent surface smoothness for lower microwave losses. All these attributes make glass an excellent candidate for 5G substrate applications. Glass with low-loss epoxy was chosen as the front-up candidate material.

Glass test-vehicles with CBCPW transmission lines of various lengths were designed and fabricated. The modelling of transmission lines is based on glass TV and the same lengths are used on other decided combinations of substrates. The simulations were performed using ADS software from Keysight Technologies. The simulation data is compared with the measured results from glass TV to analyze if the insertion loss goal of 0.05 dB/mm could be achieved. If the transmission line length is a fraction of the wavelength, losses from launching and radiation can overshadow that of the transmission line itself. Therefore, another set of simulations is performed with increased line length as compared to glass TV to get a better set of results for insertion loss. The measured results are tabulated as mean and worst-case losses in dB/mm for all three CBCPW lengths. The responses are spread across a standard deviation of 7.32% in case of shortest length of TL, which indicates a high level of consistency in the measurement data. Simulation data from laminate core also shows promise to achieve low loss at mm-wave frequencies.

5.2 Model-to-Hardware Correlations with glass 5G substrates

One of the tasks of this research is to investigate model-to-hardware correlations and identify the reasons for discrepancy. A rectangular patch antenna is chosen as a test structure as antenna design for 5G bands. HFSS by ANSOFT was used for the modeling. The antennas are designed at 37.5, 38, 38.5 and 39 GHz with 20 coupons of each antenna on the same mask. The structures were fabricated using standard semi-additive patterning process. The antennas are tested for their resonance frequency. The results are compared with the simulations and the discrepancy is explained in terms of the dimensional variations during the fabrication process, uncertainties in the thickness, and deviations between the assumed and actual electrical properties. Measurements errors from probing at mm wave frequencies are also studied.

5.3 Conclusion and Future Work

- Emerging low-loss dielectrics need to be investigated in detail and evaluated for mm-wave applications, processability and stability of electrical properties with frequency
- Innovative transmission line designs should be explored for better insertion loss measurements and reduce the contributions from high-frequency parasitics
- Process tolerance needs to be improved to below 2% for better impedance control and model-to-hardware correlations
- The effect of via transitions in buildup layers and its contributions to losses, impedance match or VSWR need to be studied in detail

Model-to-Hardware Correlation Study

- In-house characterization of electrical properties of recommended substrates should be performed upto 100 GHz
- Design and fabrication of high-gain and wide-bandwidth antennas on ultra-thin substrates should also be supported with model-to-hardware correlation study
- The sensitivity of antenna performance to geometries and materials properties should be quantified to identify the origin of discrepancy between model and hardware

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